Self-Diagnosis Implantable Optrode for Optogenetic Stimulation

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Abstract

As a cell type-specific neuromodulation method, optogenetic technique holds remarkable potential for the realisation of advanced neuroprostheses. By genetically expressing light-sensitive proteins such as channelrhodopsin-2 (ChR2) in cell membranes, targeted neurons could be controlled by blue light. This new neuromodulation technique could then be applied into extensive brain networks and be utilised to provide effective therapies for neurological disorders.

However, the development of novel optogenetic implants is still a key challenge in the field. The major requirements include small device dimensions, suitable spatial resolution, high safety, and strong controllability. In particular, appropriate implantable electronics are expected to be built into the device, accomplishing a new-generation intelligent optogenetic implant. To date, different microfabrication techniques, such as wave-guided laser/light-emitting diode (LED) structure and μLED-on-optrode structure, have been widely explored to create and miniaturise optogenetic implants. However, although these existing devices meet the requirements to some extent, there is still considerable room for improvement.

In this thesis, a Complementary Metal-Oxide-Semiconductor (CMOS)-driven μLED approach is proposed to develop an advanced implantable optrode. This design is based on the μLED-on-optrode structure, where Gallium Nitride (GaN) μLEDs can be directly bonded to provide precise local light delivery and multi-layer stimulation. Moreover, an in-built diagnostic sensing circuitry is designed to monitor optrode integrity and degradation. This self-diagnosis function greatly improves system reliability and safety. Furthermore, in-situ temperature sensors are incorporated to monitor the local thermal effects of light emitters. This ensures both circuitry stability and tissue health. More importantly, external neural recording circuitry is integrated into the implant, which could observe local neural signals in the vicinity of the stimulation sites. Therefore, a CMOS-based multi-sensor optogenetic implant is achieved, and this closed-loop neural interface is capable of performing multichannel optical neural stimulation and electrical neural recording simultaneously. This optrode is expected to represent a promising neural interface for broad neuroprosthesis applications.

Publications

Patents

1. Degenaar P and **Zhao H**, “Implantable Optrode”, Application No.: GB1410886.4, Filed by Intellectual Property Office, UK, Filing Date: 18 June 2014.

2. Degenaar P and **Zhao H**, “Optical Stimulation Arrangement”, Application No.: GB1616725.6, Filed by Intellectual Property Office, UK, Filing Date: 30 Sep 2016.

On-going Journal Papers

3. **Zhao H**, Sokolov D, Degenaar P, "A CMOS-based Implantable Optogenetic Stimulator with Self-Diagnosis Function", *IEEE Transactions on Circuits and Systems I: Regular Papers*, (ready to submit), Jan 2017.

4. "An Integrated Optogenetic Implant for Closed-Loop Neural Optical Stimulation and Electrical Recording", *IEEE Transactions on Biomedical Circuits and Systems*, (finalising draft), Jan 2017.

Published International Conference Papers

5. **Zhao H**, Sokolov D, Degenaar P, "An Implantable Optrode with Self-Diagnostic Function in 0.35μm CMOS for Optical Neural Stimulation", *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2014 (***Best Paper***).

6. **Zhao H**, Liu Y, Constandinou TG et al., "A CMOS-based Neural Implantable Optrode for Optogenetic Stimulation and Electrical Recording", *IEEE BioCAS*, 2015.

7. Soltan A, **Zhao H**, Chaudet L, et al., "An 8100 Pixel Optoelectronic Array for Optogenetic Retinal Prosthesis", *IEEE BioCAS*, 2014.

Local Conference Papers

8. **Zhao H**, Sokolov D, Degenaar P, "An Integrated Closed-loop Neural Interface for Focal Epilepsy", *UK Sensory Motor Conference*, 2016.

9. **Zhao H**, Sokolov D, Degenaar P, "Design and Implementation of a CMOS-based Brain Implant for Neuroprosthesis", *Newcastle Annual Research Conference*, 2015 (***Best Paper***).

10. **Zhao H**, Sokolov D, Degenaar P, "A CMOS-MEMS based Feedback-loop Microsystem for Implantable Biomedical Applications", *North East Epilepsy Research Network Meeting*, 2013.

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List of Acronyms

AC	Alternating Current
AlGaP	Aluminium Gallium Phosphide
ADC	Analogue to Digital Converter
CAN	Controller Area Network
CANDO	Controlling Abnormal Network Dynamics using Optogenetics
ChR2	Channelrhodopsin-2
CMOS	Complementary Metal-Oxide-Semiconductor
CNS	Central Nervous System
CT	Computed Tomography
CUP	Circuit under Pad
DAC	Digital to Analogue Converter
DBS	Deep Brain Stimulation
DEMUX	Demultiplexer
DRIE	Deep Reactive-Ion Etching
ESD	Electrostatic Discharge
FDA	Food and Drug Administration
FPGA	Field-Programmable Gate Array
FSM	Finite State Machine
GaAs	Gallium Arsenide
GUI	Graphic User Interface
GaN	Gallium Nitride
HaloR	Halorhodopsin
IC	Integrated Circuit

IPD	Inorganic Photodetector
LED	Light-Emitting Diode
LFP	Local Field Potential
LGN	Lateral Geniculate Nucleus
LMP	Low Melting Point
LNA	Low Noise Amplifier
MEA	Microelectrode Array
MHRA	Medicines and Healthcare Products Regulatory Agency
MOSFET	Metal-Oxide-Semiconductor Field-effect Transistor
MUX	Multiplexer
NpHR	Natronomas pharaonis HaloRhodopsin
OPA	Operational Amplifier
PCB	Printed Circuit Board
PCD	Polycrystalline Diamond
PI	Polyimide
PMT	Photomultiplier Tube
PNS	Peripheral Nervous System
PTAT	Proportional To Absolute Temperature
P-to-S	Parallel to Serial Interface
PWM	Pulse Width Modulation
RP	Retinitis Pigmentosa
SAR	Successive Approximation Register
SEM	Scanning Electron Microscope
S-to-P	Serial to Parallel
SPAD	Single-Photon Avalanche Diode
SPI	Serial Peripheral Interface
S-R	Set-Rest
SRAM	Static Random-Access Memory

STN	Subthalamic Nucleus
TCA	Trans-Conductance Amplifier
TLE	Temporal Lobe Epilepsy
UART	Universal Asynchronous Receiver/Transmitter
WHO	World Health Organization

To my beloved family

Yu, Li, and Sun

1 Introduction

1.1 Motivation

Over the last few decades, neurological disorders have become one of the greatest challenges to public health. The World Health Organization (WHO) has estimated that more than one billion people have been affected by neurological disorders and their sequelae [1, 2]. Recent advances in the development of neuroprosthetic devices open a new door for treatments of neurological disorders and psychiatric illnesses. In recent years, significant progress has been made in the field of neuroprosthetics. A typical application is deep brain stimulation (DBS), which has been applied to provide effective therapies for several neurological disorders, including Parkinson's disease, dystonia, and essential tremor [3, 4]. Another very successful application is the cochlear implant. More than 324,000 patients have used this type of neuroprosthetic device to recover their sense of hearing [5-8]. Despite the success of these mature techniques, it is very difficult to apply them in extensive brain networks and complex neural circuits. This is mainly due to the lack of cell-specific targeting capabilities. Hence there is an increased need to develop a cell-specific neuromodulation technique.

With the discovery of ChR2, a new therapeutic approach to neurological disorders called optogenetics has been identified. This method could provide specific-cell-type targeting neuromodulations by photosensitizing neurons through opsin expressions. Single neuron or specific neuron populations could then be activated or inhibited by predefined light emissions. This emerging neuromodulation technology can be fully applied in the investigation of complicated brain networks and neurological disorders. Over the past ten years, many studies of biomedical applications using optogenetics have been conducted. In 2005, Boyden *et al.* [9] conducted an *in-vitro* experiment to activate hippocampal neurons via ChR2. An incandescent lamp with 450-490 nm wavelength and 300 W power was utilised along with a Chroma excitation filter for optical neural stimulation, while a whole-cell patch clamp was incorporated to record the light-induced neural signals. In 2007, Aravanis *et al.* [10] reported the first work of optogenetic modulation applied to a whole animal brain. A fibre-coupled laser

diode system (473 nm wavelength, 20 mW power) was utilised to stimulate the motor cortex of living rodents. Thereafter, many optogenetic implants have been constructed for studies of optical neural activities and behaviours. Since optogenetics holds significant potential to provide effective treatments for neurological disorders, there is a growing demand for the development of new types of optogenetic implants. The requirements here primarily include multi-site stimulation, programmable intensity controllability, safe operation, and miniaturisation. To date, various development techniques have been explored to create and miniaturise optogenetic implants. One commonly-used approach is the wave-guiding laser/LED structure. Although these methods can fulfil the requirements to some degree, it is difficult to multiplex their light sources for multi-site stimulation. In addition, these devices need dedicated optical fibres and communicators, which may somewhat limit their applications for freely-moving animal experiments. Another topology for optogenetic implant designs, the μLED-on-optrode structure, has also been studied recently. This structure can accomplish multi-site stimulation via the direct insertion of light emitters into the brain area of interest. However, this method might induce thermal dissipation in local tissues. Moreover, this type of device usually requires an external controlling system for implant manipulation, adding further constrains for freely-moving animal experiments and increasing costs. Besides this, most of these existing devices are custom-fabricated, which is cost-inefficient and labour-intensive as well as challenging for other researchers to adopt.

Thus, a successful optogenetic implant should meet diverse technical requirements from different aspects. For biological applications, the implant should be able to achieve targeted-depth tissue penetration with accurate light delivery. Meanwhile, it is highly desirable to obtain multi-site/multi-layer stimulation operations in accordance with the six cortical layers. More importantly, safety is always paramount for implantable applications. The integrity, long term durability, and thermal effects of the device need to be comprehensively assessed in order to ensure implant stability and tissue safety. For the device itself, intelligent implantable electronics are demanded to be built inside of the implant, rather than incorporating external costly/bulky control instruments. The controlling system should be fully compatible with standard neurological pacemakers/bio-medical processors. The implant should also be manufactured using the commercially available fabrication

process. This could not only save on costs but would also provide feasibility for wider applications. In term of electronics design, strong light intensity controllability should be attained by constructing specific electronic components. This would be beneficial for stimulation efficiency/accuracy and thermal management. Furthermore, dedicated sensing circuitries need to be developed so as to realise real-time integrity and operational degradation assessment and thermal monitoring. Moreover, external electrical neural recording circuitry should be able to be integrated into the optogenetic implant, accomplishing an advanced closed-loop optical-electro neural interface.

1.2 Research Aim and Objectives

The aim of this research is to develop a new type of optogenetic implant (optrode) using a CMOS-driven GaN μLED approach which addresses the above challenges. This design is intended to facilitate effective gene therapies for common neurological disorders and brain illnesses. Multifunctional operations could be achieved within a single optrode (optical probe), including optical neural stimulation, electrical neural recording, diagnostic sensing, and thermal monitoring.

The primary objectives of this research are:

- To propose a conceptual design for the targeted implant.
- To analyse and define the main design specifications, in terms of the controlling scheme, fabrication technology, light-driving ability, luminance intensity controllability, long term durability assessment, thermal management, in-situ sensing mechanisms and electrical recording.
- To investigate and develop suitable electronic μLED drivers for targeted optogenetic activations and future exploration.
- To incorporate different modulation methods to achieve outstanding and highly programmable light intensity modulation.
- To explore and implement specific electronic elements for multi-site/multi-layer local light delivery.
- To create a self-diagnosis scheme to assess optrode integrity and operational degradation.

- To investigate and implement specific electronic components for diagnostic sensing circuitry.
- To analyse and integrate local temperature sensors into the proposed optrode.
- To incorporate external existing neural recording circuitry into the proposed optogenetic implant.
- To characterise and validate fabricated optogenetic implants.

1.3 Thesis Outline

This thesis is structured as follows:

Chapter 2 briefs the relevant backgrounds and reviews the state of the art of optogenetic implants. The fundamentals of neuroprosthetics are firstly introduced. Then the basics of optogenetics are described, in which the rationale and related applications of optogenetic stimulation are explained. The focus then moves onto the current state of development of optogenetic implants, and recently published work is reviewed and compared. In the end, the demand for a new type of optogenetic implant is justified, along with associated development criteria.

Chapter 3 depicts the main design specifications of the proposed CMOS-driven μLED optogenetic implant. This implant could achieve multifunctional operations, including optical stimulation, diagnostic sensing, temperature sensing, and electrical recording. This chapter elaborates on the major development requirements, providing clear standards for both circuit design and system implementation.

Chapter 4 details the specific circuit designs for optical stimulation and diagnostic sensing, including the μLED driver, pulse width modulator, amplification stages, data converters, and related accessory cells. Different versions of designs are proposed, compared and implemented respectively, and this chapter provides a comprehensive components library for system implementation.

Chapter 5 presents the system implementation of the proposed optogenetic implant using circuit components developed in Chapter 4. Both open-loop and closed-loop implantable optrodes have been constructed, verified and compared. Optical stimulation, diagnostic sensing, thermal sensing and electrical recording are

realised in the proposed optrode, achieving a novel multifunctional optogenetic implant.

Chapter 6 concludes the content of this thesis and also looks at potential future work.

2 Background and Literature Review

2.1 Introduction

The brain is a complex organ, containing billions of interconnected nerve cells with vastly different sizes, shapes, activities and wiring patterns. In the past decades, based on the considerable effort and significant progress of neuroscientists and neuro-engineers, diverse electrical neuromodulation techniques have been developed and widely applied for neural prostheses and therapies [11-15]. In 2003, with the finding of ChR2, a new neuromodulation technique called optogenetics was created. This gene-based optical technology can photosensitize neurons through ChR2 or other types of photosensitive proteins, and these neurons can then be manipulated by light. This cell-specific optical technique can be employed to investigate complex brain networks, and it holds remarkable potential for neurological disorder therapies. Thus, there is a growing demand to construct advanced optogenetic implants which can precisely and reliably deliver light into targeted areas of brain tissue.

In the following two sections, the fundamentals of neuroprosthetics and optogenetics are described. In section 2.4, state-of-the-art development techniques for optogenetic implants are reviewed. This chapter then summarises the key development criteria for optogenetic implants.

2.2 Background on Neuroprosthetics

2.2.1 Concept

In recent decades, neurological disorders have affected people worldwide. Based on the estimation from the WHO, more than 6.8 million people are died every year due to neurological disorders [1, 2]. Thanks to the advances of neural modulation methods, the field of neuroprosthetics has been rapidly developed. Neuroprosthetics are a class of (implantable) devices which can be utilised to restore, replace or improve lost or damaged nervous functions caused by neurological disorders [13]. It usually consists of a stimulator module to which delivers stimulating or inhibiting signals to (or near to) the targeted tissue via voltage, current and/or other modalities.

In recent years, neural recording elements have increasingly been incorporated into the neuroprosthetic systems for the observation and monitoring of neural activities [12-14].

Neuroprosthetics can be divided into different categories: motor prosthetics, sensory prosthetics, central nervous system (CNS) pacemakers, and peripheral nervous system (PNS) pacemakers [13, 16-18]. In recent decades, researchers have explored various approaches to these prosthetic applications.

2.2.2 Applications

Motor Prosthetics

The term motor prosthetics generally refers to those neuroprosthetic devices which could restore a patient' motor functions from the autonomous nervous system. A typical application of motor neuroprosthetics is bladder prostheses. For patients who have paraplegia owing to spinal cord lesions, entirely emptying the bladder may be problematic, and this could result in severe infections. In 1987, the first successful human trial of a sacral anterior root stimulator was performed [19]. It delivered intermittent stimulation to the sacral anterior root ganglia, and consequently enhanced the bladder emptying function of patients. Since then, several studies have been conducted to achieve better device performance [20-22]. Figure 2.1 shows the bladder control implant which has generally been applied for medical use in recent years.

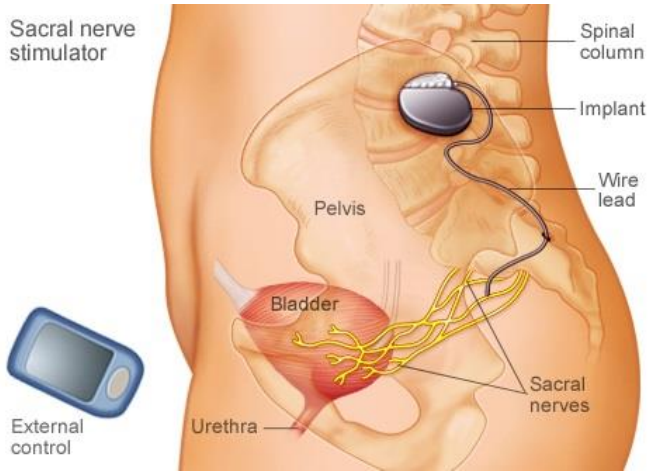


Figure 2.1 A bladder prosthesis system which has been widely used for medical treatment [22]. The system mainly consists of a sacral nerve stimulator and an external controller. The stimulator is typically implanted through a miniature cut above the tailbone via surgery, and it can stimulate the sacral nerves which dominant bladder functioning.

Sensory Prosthetics

The focus of sensory prosthesis is to use specific devices to bring back the sensing functions of patients, such as auditory prosthetic and visual prosthetic. Auditory prosthesis mainly consists of three modalities: the cochlear, auditory midbrain and auditory brain implants [23, 24]. This categorisation is determined by the location of the implant. The cochlear implant is implanted into a patient' cochlea; the targeted neuron population of auditory midbrain stimulation is the auditory nerve cells in the inferior colliculus; and the functioning area for auditory brain implant is in the lower brain stem. In particular, cochlear implants have become a most successful prosthetic application, not only among these three auditory prosthetics but also in all currently available neuroprosthetic devices. The first type of cochlear implant was developed in 1973 and then fully approved for clinical application in 1980 [5, 25]. These implants have been utilised by over 324,000 patients to restore their sense of hearing [5-8]. A typical cochlear implant neural prosthesis system is illustrated in Figure 2.2.

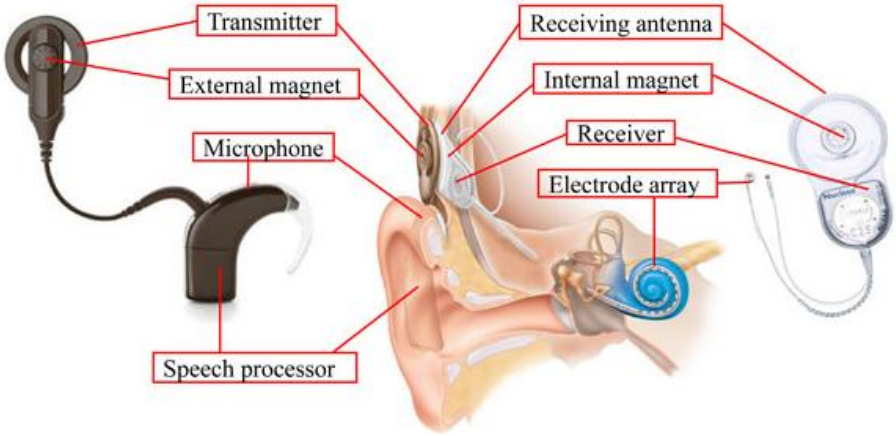


Figure 2.2 Typical diagram of cochlear implant neural prosthesis system [8]. It uses external recording components to receive sound waves. Next, recorded sound information is wirelessly transmitted into implanted electrodes. These electrodes could then stimulate the targeted neurons, thus enabling patients to decode sound waves.

Visual prosthetics is another vital sensory prosthetics application. Researchers have adapted the common knowledge and techniques which utilised for cochlear implants into visual prostheses [26, 27]. A visual prosthetic device can develop and deliver image information by electrically or optically stimulating targeted visual neurons. Although specific prosthetic components may vary, the visual prosthetic system usually consists of four modules [28]. Firstly, an external video camera

would be used for recording the image. The second part is a signal processor which receives and decodes the input image information and then generates and conveys corresponding operation instructions to the output stage. The third module is the output stage, where a neural (implantable) stimulator is activated to stimulate targeted visual nerve cells via either voltage modality or light modalities. The final part is the system power supply, where either a portable battery or wireless power transmission is used. A general conceptual diagram of the visual prosthesis is illustrated in Figure 2.3.

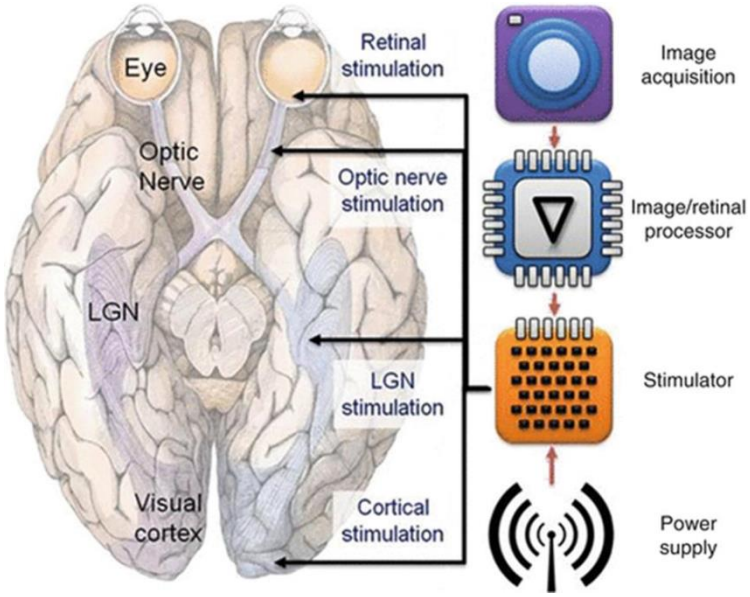


Figure 2.3 General conceptual diagram of visual prosthesis [28]. Visual prosthetic systems usually consist of four main modules: image acquisition stage, image processing, neural stimulator, and power supply.

Visual prosthetic devices can be classified into four categories: retinal prosthesis, visual thalamic prosthesis, visual cortex prosthesis, and optical nerve prosthesis [28-30]. And this depends on where the stimulator is positioned in the visual pathway. The neural stimulator of retinal prosthesis is placed into the retina, whereas in a visual thalamic prosthesis it is located at the lateral geniculate nucleus (LGN) of the thalamus. The implant for visual cortex prosthetic is inserted into the visual cortex. And an optical nerve prosthesis is fitted in the optical nerve, as an intermediate method between retinal neuroprosthetics and visual cortex prosthesis. Figure 2.4 depicts a novel optogenetics retinal prosthesis system.

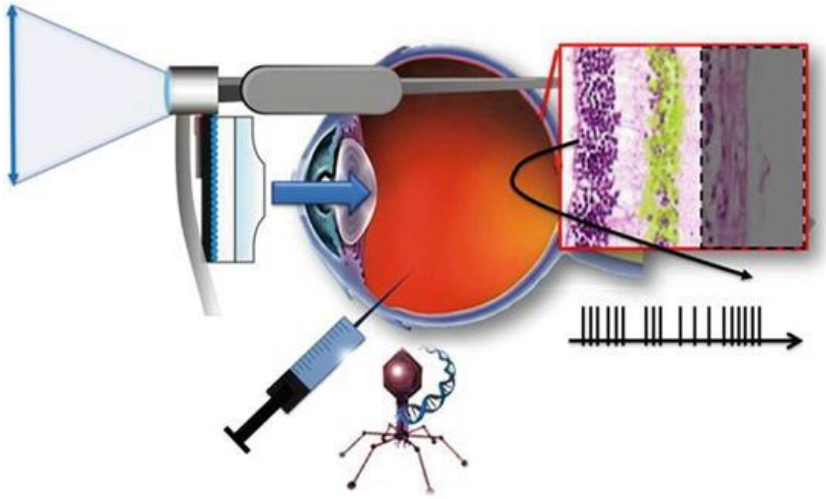


Figure 2.4 Diagram of an optogenetics retinal prosthesis system [28]. A specific virus is injected into the eye to photosensitize retinal cells. A high-density optical array could be utilised to project light pattern into the eye.

Peripheral Nervous System (PNS) Pacemakers

A PNS pacemaker is a battery-powered device used to deliver a stimulus for PNS neuromodulation. A commonly utilised type of PNS pacemaker is the heart pacemaker. It senses the abnormal heart rate a of patient and then adjusts the heart rhythm into a normal range [31, 32]. A heart pacemaker mainly consists of two parts, a pulse generator and a pacemaker lead, as shown in Figure 2.5. The pulse generator produces the pulse signals to regulate the heart rhythm, and a battery is embedded to power the pacemaker; the pacemaker lead connects the pacemaker to the heart and transmits the pulse signals to it.

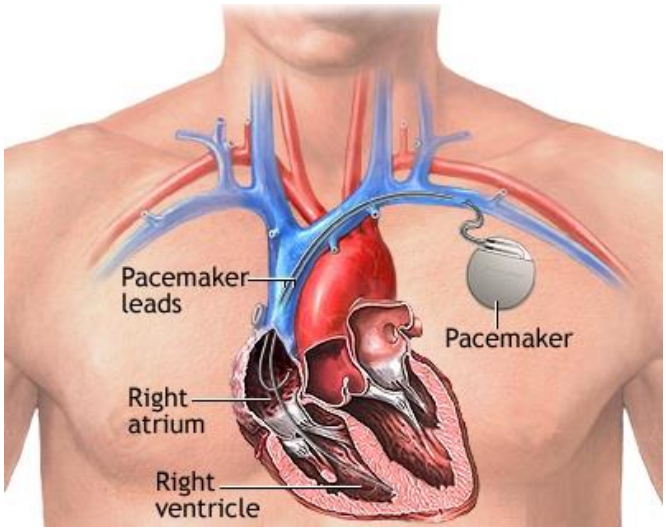


Figure 2.5 A commonly-used heart pacemaker system [31]. The pulse generator is placed at the chest, and the pacemaker lead transfers the electrical pulses from the pacemaker to the heart.

Central Nervous System (CNS) Pacemakers

A CNS pacemaker is usually a chest device to generate electrical pulses for CNS neuromodulation. A very successful application related to CNS pacemakers is DBS. This technique has been widely utilised for various types of neurological disorders and brain illnesses such as Parkinson's disease, dystonia, and essential tremor [3, 4]. A typical DBS prosthetic device is illustrated in Figure 2.6. For this standard DBS system, electrodes are placed into the targeted area of brain tissue (such as the subthalamus nucleus) using a stereotactic localising system. And the pulse generator acts as a pacemaker to inject and control the pulse. Usually, the clinician/patient defines the pulse duration and amplitude [3, 33].

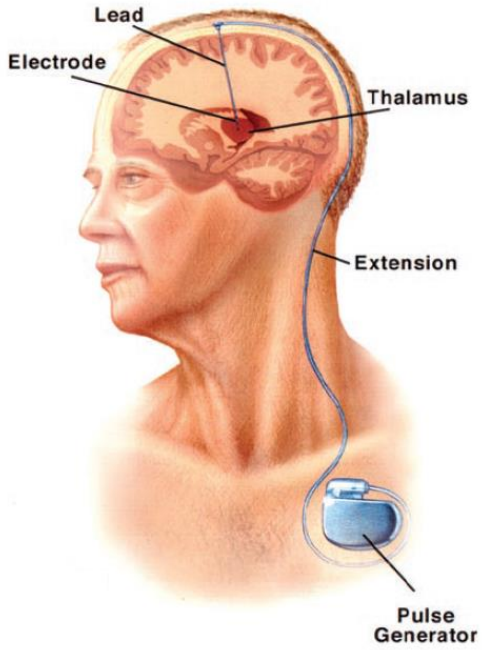


Figure 2.6 A typical DBS system[3]. This system mainly consists of an electrode, a bio-compatible lead with extension, and the pulse generator.

Closed-loop Prosthetics

In order to enhance the accuracy and efficiency of DBS systems, a closed-loop mechanism has been investigated [34]. And then closed-loop methods have also been studied for use in therapy for epilepsy [35-38] and other diseases [39-42]. In recent years, efforts have increasingly been focused on incorporating closed-loop strategies into diverse neuroprosthesis applications [43-47]. Even though open-loop control schemes have been widely utilised for most commercial neuroprosthetic devices, there are several merits of closed-loop neural systems, in terms of device capability,

operational effectiveness, functioning accuracy, and power efficiency [34, 43, 46]. It can thus be predicated that closed-loop integration will be a trend in future neuroprosthetic device development.

2.2.3 Summary

The research of the neuroprosthetics takes place at the cutting-edge of engineering and science. In the past decade, the field of neuroprosthetics has attracted close attention among neuroscientists and neural engineers. This evolving technology is continuously being pushed forward by neural engineers, and the impact would be paramount for both area of research and general society.

2.3 Background on Optogenetics

2.3.1 Concept

Optogenetics is an emerging neuromodulation technique that can render neurons controllable by light. This technique combines genetic and optical methods to activate or inhibit specific neurons. Even though optogenetics is a comparatively fresh technique, using a light source to control neurons is not a brand-new idea. A very early application of optical neural stimulation was conducted in 1971 [48]. For the first time, blue light was utilised to accomplish targeted neural stimulation, and action potentials in Aplysia ganglia were successfully triggered. In 1999, Nobel laureate Francis Crick proposed the rudiment of optogenetics: a new optical method which could be used to trigger or silence specific types of neurons without any influence on other neuron populations [49].

Over the past two decades, numerous optical stimulation tools have been developed [50-55]. However, since these tools are mainly based on either the utilisation of exogenous cofactors or the expression of multiple proteins, they are difficult to be employed into *in-vivo* applications [56]. In 2003, the expression of a single photosensitive protein, ChR2, was discovered [57]. It can be transgenically expressed into neurons, and then these neurons could be depolarised with light illumination [9]. After that, the new type of optogenetic technology was founded. This light-sensitive cation channel has been employed to realise precise spatial-temporal control of neuronal activities both *in vitro* [9, 58] and *in vivo* [10, 59-62].

While ChR2 is utilised to enable neurons with specific behaviour, there is also a need to develop a different tool which can silence neurons for a particular action. In 2007, a chloride pump, halorhodopsin (HaloR, also called NpHR for *Natronomas pharaonis* halorhodopsin), was revealed from the archaebacterium *Natronomas pharaonic* [63]. This pump allows neurons to be hyperpolarised by yellow light, and then specific neuron behaviours could be inhibited with particular light illuminations [63-65]. Since then, the field of optogenetics has been fully established, and this technique has been adopted to explore complicated brain circuits and neurological illnesses [66-70]. Figure 2.7 demonstrates the basic working principles of optogenetics stimulation using ChR2 and NpHR.

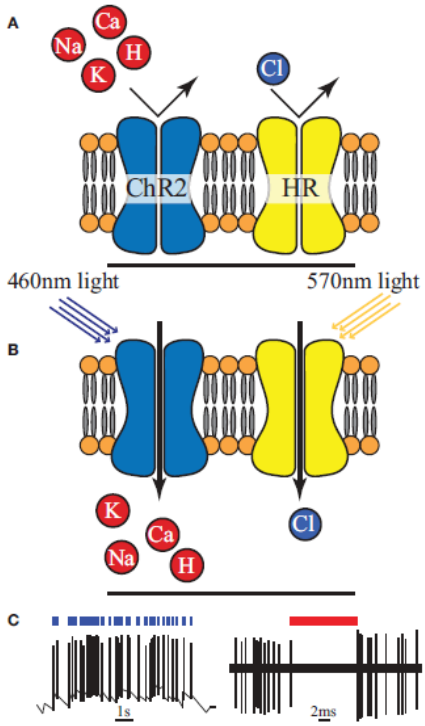


Figure 2.7 A principle diagram of optogenetics stimulation using ChR2 and NpHR [11]. (a) The ChR2 ion channel and NpHR ion pump are both in inactive states. (b) After receiving blue/yellow light (with predefined wavelength), positive ions and chloride ions enter the cell via ChR2 and NpHR respectively. (c) ChR2 activation triggers action potentials, while action potentials are inhibited by the activation of NpHR.

2.3.2 Applications

Although optogenetics is still a relatively new technology, the exploration of clinical applications using optogenetics has rapidly progressed. An advantageous application is to employ optogenetics for the analysis of disease principles and treatment mechanisms. In 2009, a ChR2-NpHR optogenetic system was developed

based on a fibre-coupled laser diode [71], as shown in Figure 2.8. This optical device was implanted into freely moving rodents which were parkinsonian. By applying selective light stimulation/inhibition to corresponding afferent axons, the therapeutic effects of DBS within the subthalamic nucleus (STN) were inspected. This system provided a deep understanding of DBS mechanisms. It also indicated that optogenetics can be an effective tool in analysing unhealthy brain circuitry.

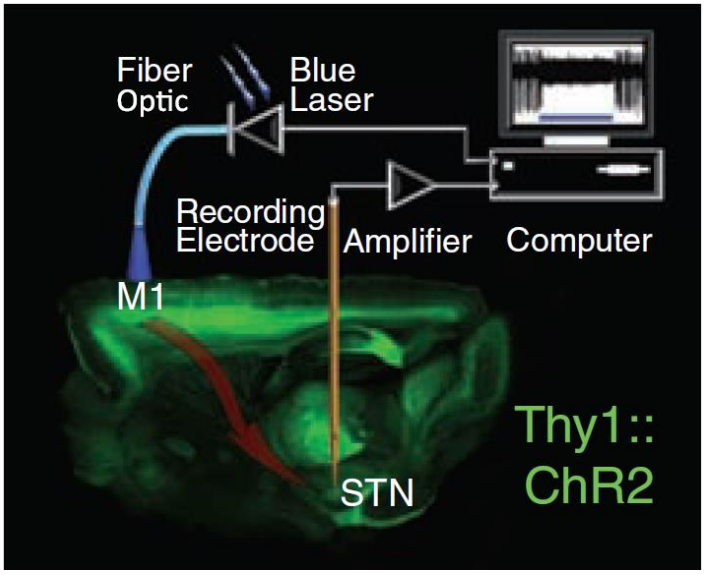


Figure 2.8 Simplified diagram of the ChR2-NpHR optogenetics system[71]. A fibre-coupled laser is used for light activation and inhibition. A recording electrode observes the neural signals from the STN, and these signals are then sent to a PC console after amplification.

In addition to Parkinson's disease, optogenetic techniques have also been utilised in studying other brain illnesses. In 2012, a closed-loop optogenetics system was developed for temporal lobe epilepsy (TLE) treatment [72], as shown in Figure 2.9. This system was applied into an epileptic mouse model. When the seizure was observed by the system, the real-time detection algorithm then triggered the optical stimulator to deliver specific light into targeted neural populations. NpHR and ChR2 were both incorporated to inhibit and stimulate two different types of hippocampal nerve cells simultaneously. This cell type-specific method demonstrated a finer seizure controllability for TLE.

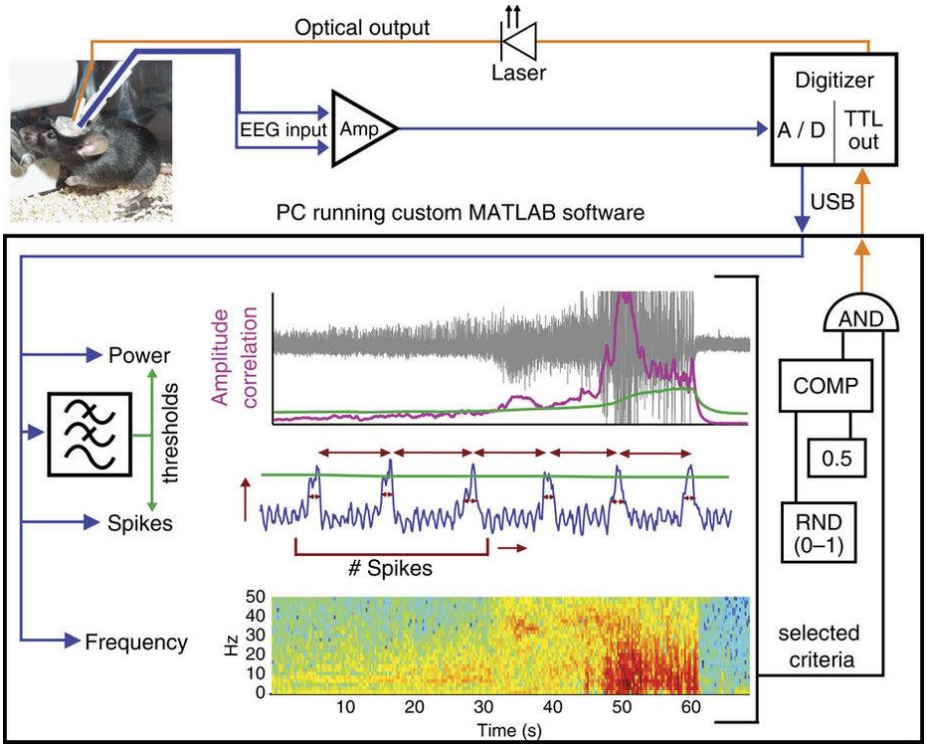


Figure 2.9 Closed-loop optogenetics system for TLE [72]. EEG signals are recorded from the hippocampus area of the mouse. These are sent to a PC-based seizure detection software via amplification and A-D conversion stages. The PC console could then determine whether to trigger the optical stimulator.

Moreover, optogenetic techniques have also been applied for visual prostheses. In 2006, the ChR2 expression was imported into the retinal ganglion cells of experimental mouse, in which the photoreceptors had been mostly degenerated [73]. After importation, the retinal ganglion cells were able to code light signals. Subsequent clinical explorations were then conducted. In 2014, the US Food and Drug Administration (FDA) granted clinical trials in patients with retinitis pigmentosa (RP) [74]. In March 2016, the RP RST-001 project performed an optogenetic clinical trial, and successfully completed the first patient experiment [75, 76]. This was the first optogenetic clinical trial ever in the world. With this emergence of the first clinical trial using optogenetics, further attempts of optogenetic clinical applications are expected to be conducted in near future [77].

2.3.3 Summary

As a novel neuromodulation tool, optogenetic approaches have been widely investigated and applied for typical neurological disorders, such as Parkinson's disease [71, 78], epilepsy [72, 79, 80], visual prosthesis [65, 66, 73-76, 81] and other

diverse illnesses [10, 70, 82-87]. Further opportunities for optogenetic applications are emerging in the broad neuroscience community. In the meantime, it also indicates an increasing request for engineers, which is to construct more advanced engineering tools for optogenetic stimulation.

2.4 Literature Review of Optogenetic Implants

2.4.1 Introduction

As a cell type-specific neuromodulation method, optogenetics opens a new door for neuroprosthesis applications. In the past decade, neuroscientists have discovered numerous light-gated microbial opsins to activate, inhibit or bi-directionally manipulate targeted neuron populations [57, 63, 88, 89]. In particular, the advance of ChR2 and NpHR makes relatively low-intensity optical neuromodulation possible [88, 90]. They only require less than 1 mW/mm^2 (ChR2) or 7 mW/mm^2 (NpHR) light intensity to reach the threshold. Owing to this merit, many biological experiments (*in-vitro* or *in-vivo*) have been performed to investigate complex brain circuitry and chronical brain illnesses, as described in Subsection 2.3.2.

Hence, there is an increasing need to construct novel optogenetic implants, using appropriate engineering approaches. These implants should be able to achieve precise light emission, and to reliably deliver light to targeted areas of brain tissue. Besides this, they should be capable of being applied in large brain circuitries for multi-site and multi-layer operations. They should also hold reasonable spatial resolution and suitable light intensity controllability. In particular, each stimulation site should be accessed and manipulated individually. In addition, it is desirable and meaningful to integrate neural recording electronics into these implants for closed-loop neuroprosthetics. Lastly, it would be advantageous if relevant safety and durability evaluation scheme can be created for these implantable devices.

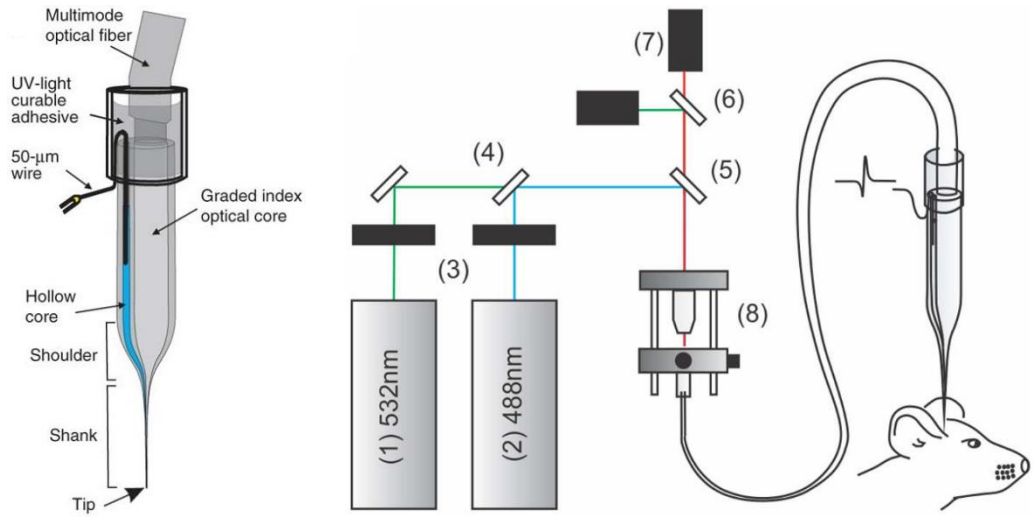
In this section, the state of the art of optogenetic implants is reviewed. The current achievements in optogenetic implant developments are highlighted, and their limitations are also identified. Based on different methods used for light delivery, optogenetic implants can be classified into two categories: wave-guided structure and direct μLED-on-optrode approach. An optical waveguide is a physical component applied for light confinement and transmission [91]. A typical optical waveguide

element is an optical fibre, and it has been commonly utilised for light coupling. In the μLED-on-optrode structure, μLEDs are selected as the light source. Rather than cooperating with waveguide elements, these μLEDs are directly bonded on the implant and inserted into brain tissue. In the following two subsections, these two groups of designs are introduced and compared, and their strengths and weaknesses are also correspondingly pointed out.

2.4.2 Wave-Guiding Structure

To date, different microfabrication techniques have been explored to develop advanced implantable optical stimulators. These optical implants aim to achieve local light delivery and multi-site activation with targeted luminance intensity and spatiotemporal resolution. One of the key factors for these implants is the light source. Optogenetic implants require suitable light sources which could possess sufficient light intensity and can precisely deliver light into particular area of the brain. The laser, as a well-developed illuminant, has been broadly applied into optrode developments. It can provide strong coherent light with low divergence [92, 93]. This guarantees high efficiency in light delivery. For laser-based optical implants, a wave-guiding structure is essential to be utilised for light steering [92-94]. In past few years, numerous wave-guided devices have been proposed to couple with laser sources for implantable light delivery.

In 2012, a glass fibre-coupled optical probe has been created for hybrid optical stimulation and electrical recording [95, 96], as illustrated in Figure 2.10. A single optical core is built into the probe for light emission, while a hollow core is utilised as the recording electrode. The optrode tip is formed with 10 μm diameter, and it provides single-cell resolution for light emission. A 100 nm aluminum coating is incorporated to minimise optical losses during light delivery. The maximum light intensity is around 10 mW/mm^2. Shutters, dichroic mirrors, photomultiplier tube (PMT) detectors, and bandpass filters are incorporated to accomplish this optical-electrical microprobe system.



(a) (b)

Figure 2.10 (a) Schematic diagram of the multimode optical fibre-coupled probe [95]. A graded index optical core is coupled with the optical fibre to realise light delivery. A hollow core is used for the in-situ observation of neural activities. The shaft tip is shaped to 10 µm diameter for single-neuron manipulation. (b) Experiment set-up of this optical-electrical microprobe system [96]. (1) (2) are two different laser sources; (3) are two shutters; (4) (5) (6) are dichroic mirrors; (7) are PMT detectors and bandpass filters; (8) is a fibre optical launch system.

This optical probe holds several advantages. First of all, it possesses a very small probe tip. This facilitates the manipulation of single neuron or small populations of neurons. It also minimises the damage to brain issue caused by physical implantation. Besides, it achieves closed-loop integration in a single probe. Nonetheless, due to the limited number of stimulation sites (only one for each shank), it is challenging to employ this device in a large brain area for multi-site and multi-layer stimulation. Moreover, it requires several external instruments to complete the experiment set-up, which increases the total system dimensions. This may not be ideal for freely behaving animal experiments or clinical applications.

Instead, a wave-guiding optrode-MEA (microelectrode array) system has been developed for concurrent optical stimulation and electrical recording [97]. This design is constructed based on a 6×6 Utah MEA; wherein one microelectrode is substituted by a fibre-coupled optical probe. A system overview diagram is illustrated in Figure 2.11. The length of each microelectrode shank is 1 mm, and the pitch between every two microelectrodes is 400 µm. This optrode-MEA array achieves single site stimulation and 30-channel neural recording simultaneously, in millimetres cortical region.

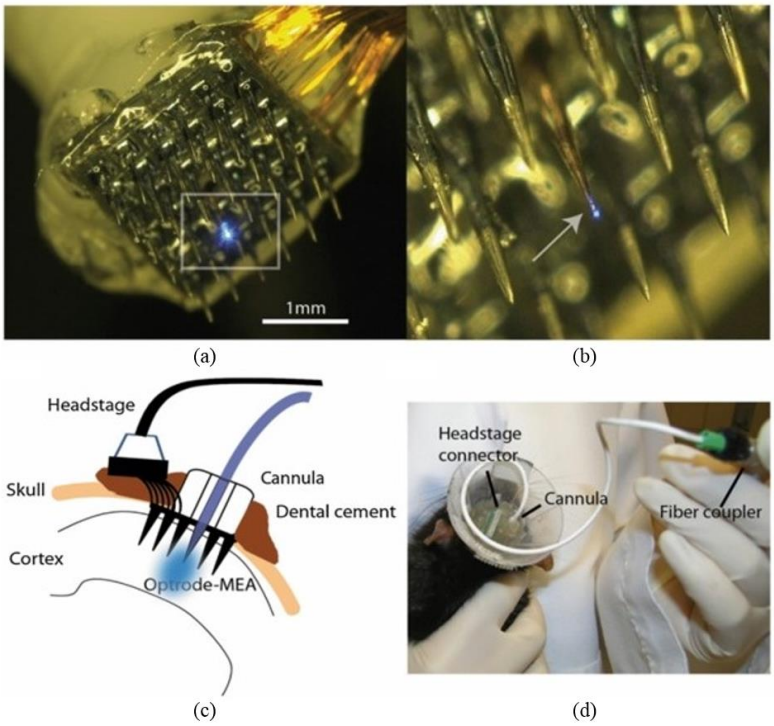
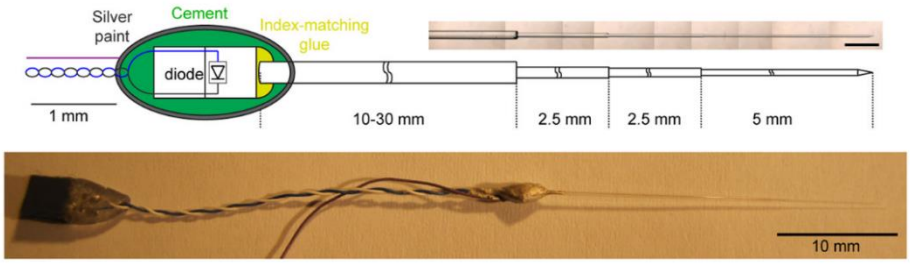


Figure 2.11 System diagram of this optrode-MEA system [97]. (a) Picture of the 6×6 Utah MEA with substituted fibre-coupled optical probe. (b) Zoom-in view of the probe tip. (c) Cartoon image of the overall system. Cannula and dental cement are used to encapsulate the optrode and MEA. (d) The system is implanted into the subject via a headstage connector.

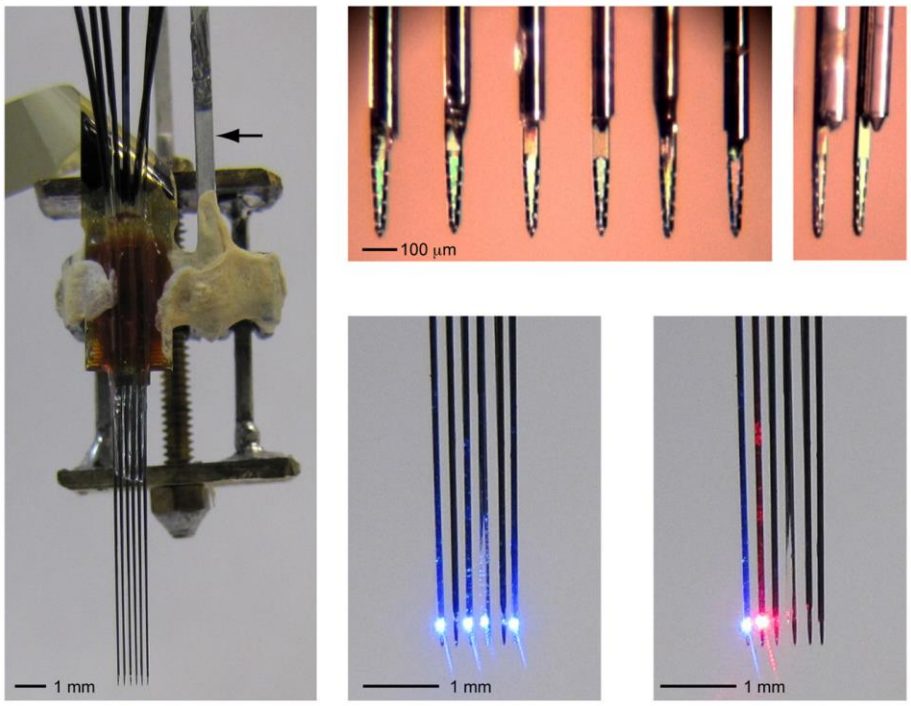
This optrode-MEA array accomplishes large-region neuromodulation. Concurrent optical stimulation and electrical neural recording are obtained. However, it can only realise single-site stimulation within each 6 × 6 array, and multi-layer stimulation is also difficult to be achieved. In addition, the fabrication process of this device is comparatively complex, which might add difficulties for other researchers' adoptions.

For the wave-guiding devices mentioned above, another concern is the laser light source. Even though laser systems can provide coherent light delivery with low divergence, there are still some areas to be improved, in terms of system miniaturisation, power efficiency, illumination stability, and operation warm-up period [92-94]. Additionally, laser systems usually require a dedicated optical interface for practical use [92, 93]. This may add extra restrictions on the freedom of experimental subjects. Another type of light source used for optogenetic stimulation is the µLED. µLEDs could potentially provide more stable light emission. Some µLEDs could also hold faster light-switching speeds with lower power consumption [92, 98]. Moreover, most µLEDs are compatible with conventional electronics for µLED driving and communication [92, 93].

Therefore, wave-guided µLED-based optical probes have drawn increasing attraction among neural-engineers. In 2012, an optical fibre-coupled multi-diode array has been developed [99]. This array consists of six individual µLED-fibre coupled assemblies. The total length of the optical fibre is up to 50 mm, containing four stepped sections. The last section is 5 mm long with a 60-70 µm diameter. A cone-shape tip is constructed with ~12° at the end of the shank. A schematic diagram is shown in Figure 2.12 (a). This single fibre assembly is duplicated by six, to construct an optical array for multi-neuron operations. The fabricated array is displayed in Figure 2.12 (b).



(a)



(b)

Figure 2.12 Fibre-coupled multi-diode optical array [99]. (a) A single four-step fibre probe. The total length is 50 mm, and the last shank is 5 mm long with a 12° tip. (b) Assembled fibre array, consisting of six individual probes with ~200 µm spacing. Four of them are designed for blue light emission, and the other two are dedicated for red light stimulation.

This fibre-coupled optical array achieves multi-site stimulation by assembling six individual probes. Besides, it also realises adjustable-depth stimulation, as the four-step probe has high flexibility for stimulation depth. But it does not achieve multi-site/multi-layer stimulation within a single probe. And the system dimensions are relatively large. Both factors could be the bottlenecks for the use of this optical array for widespread applications.

Similarly, in 2014, another fibre-coupled µLED-based optical probe has been fabricated [100], and the system overview is displayed in Figure 2.13. The µLED is flip-chip bonded on a polyimide (PI) ribbon cable. The PI cable is bendable, ensuring the flexibility of the overall system. A silicon (Si) housing is implemented to adhere the µLED to the PI cable. A 5mm-long optical fibre is fixed into a predefined recess of the Si housing to complete the system.

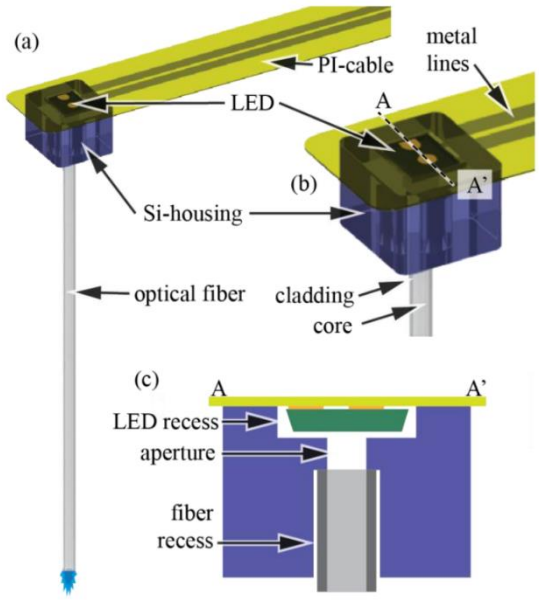


Figure 2.13 Cartoon image of the fibre-coupled µLED optical probe [100]. This system mainly consists of a 270×220×50 µm³ LED chip, a flexible PI cable, a 550×500×380 µm³ Si housing, and a 5mm-long optical fibre with 125 µm diameter.

This wave-guiding µLED-based optrode can deliver light into deep tissue areas, with the incorporation of an optical fibre. It achieves 1.71 mW/mm^2 light intensity with a 30 mA driving current and a 10% duty cycle. This meets the requirements of the ChR2 activation threshold (less than 1 mW/mm^2). Additionally, it utilises relatively straightforward fabrication techniques, which could be adapted by other researchers. But, due to the utilisation of the bulky optical fibre, it would be challenging to multiplex this optrode for multi-site operations. Besides, although the

light intensity reached the ChR2 activation threshold, it may be insufficient for higher-intensity stimulation. In addition, in order to achieve this 1.71 mW/mm^2 light intensity, the consumed power is very high.

Apart from all the devices described above, other fabrication technologies have also been explored, and diverse wave-guiding structures (both laser-coupled and LED-coupled) have been developed [101-103]. A performance summary of recently published wave-guided optogenetic implants is presented in Table 2.1. Even though these devices can meet the requirements of implantable optogenetic applications to some degree, they are still with some concerns. One limitation of some devices is that only one stimulation site could be constructed along the single probe shaft, which are not capable to be utilised for dispersed targets. In particular, due to comparatively bulky dimensions of some wave-guiding structures, the solitary light source is strenuous to be multiplexed for multi-site stimulations. For some other devices, although the single probe is duplicated into the array configuration to accomplish multi-site operations, the stimulation depth is still fixed, and multi-layer stimulation is not reachable within the single probe. This could potentially limit their applications in 3D brain network. Moreover, the light coupling efficiency of wave-guiding structures would be another limitation. Particularly for the μLED-fibre coupling efficiency, the maximum value is less than 10% [92, 104]. This may increase the system power budget and reduce the light emission efficiency. And more importantly, due to the incorporations of bulky wave-guiding structures and external optical communicators, these devices might be challenging to be applied into freely-moving animal experiments and/or clinical applications.

Table 2.1 Performance summary of recently published wave-guiding structure based optogenetic implants.

Ref.	Light Source	Dimensions	No. of Sti Sites	Max Light Intensity/Power	Max Power Consumption	Max Pulse Frequency	Electrical Recording	Fabrication Process	Substrate Material
[95]	Laser	Diameter: 200 μm Shaft tip diameter: 10 μm	1	10 mW/mm^2	N/A	N/A	Yes	Custom-Fabricated	N/A
[97]	Laser	Shaft length: 1 mm; Spacing: 400 μm	1	5 mW/mm^2	N/A	40 kHz	Yes	Custom-Fabricated	N/A
[101]	Laser	Shaft length: 7 mm; Width: 200 μm	1	N/A	21 mW (for blue light)	N/A	Yes	Custom-Fabricated	Polyimide
[102]	Laser	Shaft length: 5 mm; Width: 200 μm	1	9400 mW/mm^2	50 mW	25 Hz	Yes	Custom-Fabricated	Silicon
[103]	Laser	Diameter: 150 μm	1	0.9 mW	N/A	N/A	Yes	Custom-Fabricated	Silicon
[99]	μLED	Shaft: 5 mm; Diameter: 60-70 μm (Blue) μLED dimensions: 1.6×0.6 mm^2	1×6	40 mW/mm^2 (blue light)	Current: 60 mA	N/A	No	Custom-Fabricated	N/A
[100]	μLED	Total length: 5 mm; Diameter: 125 μm; μLED dimensions: 270×220×50 μm^3	1	1.71 mW/mm^2	Current: 30 mA	N/A	No	Custom-Fabricated	Polyimide

2.4.3 µLED-on-Optrode Structure

In addition to wave-guiding devices, another type of optogenetic implants relies on the µLED-on-Optrode structure. In this type of structure, µLEDs are straight bonded onto optical probes and distributed along the probe shaft. Then they are directly inserted into the targeted area of brain tissue. This strategy can provide higher light emission efficiency, and has the potential to realise multi-site/multi-layer stimulation within a single integral optrode. It could also free subjects from the movement restrictions caused by some bulky and cumbersome wave-guiding components.

For instance, a flexible polyimide based integrated µLED optrode has been constructed [105], as demonstrated in Figure 2.14. In this optrode, one stimulation site is created at the probe tip, surrounded by three electrode recording sites. This optical-electrical hybrid design achieves optogenetic stimulation and simultaneous neural recording within a single probe. The whole shaft length is 12 mm, and the total width is 900 µm. An off-the-shelf µLED is utilised as the light emitter, with dimensions of 1000 × 200 × 600 μm^3. The µLED drive voltage is 2.9 V, and the drive current is 5 mA. The light intensity of the µLED is fixed at 0.7 mW/mm^2.

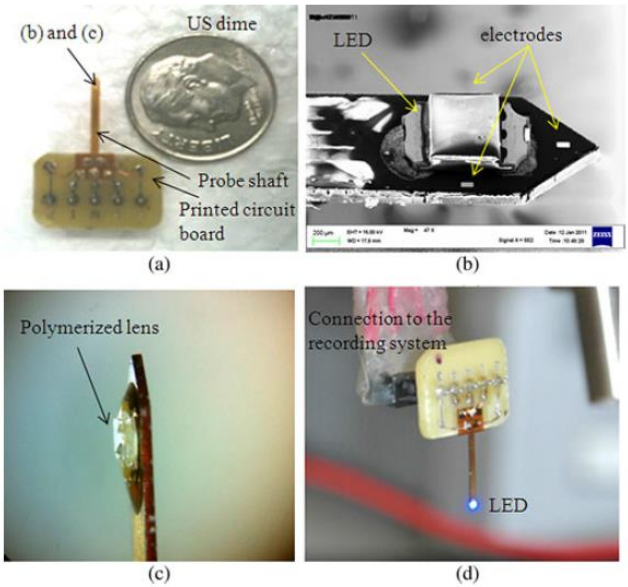


Figure 2.14 Flexible polyimide-based µLED optrode [105]. (a) A printed circuit board (PCB) is fabricated to assemble the optrode. (b) A scanning electron microscope (SEM) image of the optrode tip. The µLED site is bonded along with three recording sites. (c) A polymerised lens is covered on the µLED. (d) The overall system. µLED is turned on by a 2.9 V forward bias voltage.

This integrated μLED optrode accomplishes both optical stimulation and electrical recording. Compared to wave-guided optrodes, it is more convenient for closed-loop integration. Besides, it requires less power budget and held better compactness. Nevertheless, there are several considerations for this design. Firstly, the μLED is too bulky. This would be a bottleneck both for realising multiple stimulation sites and minimising optrode dimensions. Furthermore, heating is a key concern with the μLED-on-optrode structure, but this design does not take μLED thermal effects into account. This may potentially induce over-heating in brain tissue. Also, this design requires 14.5 mW power to achieve 0.7 mW/mm^2 light intensity, ans so that the power efficiency has some spaces for enhancement. Furthermore, the generated light intensity is difficult to activate the ChR2, whose activation threshold is ~ 1 mW/mm^2. In addition, the the optrode shaft is too long, being much longer than the average cortex thickness [106]. It may need to be shortened in the future. Moreover, the optrode width of 900 μm might damage tissue and cause neuro-inflammatory responses.

At the same period, a two-layer SU-8 based optrode has been proposed [107], and the fabricated optical probe is displayed in Figure 2.15. The total length of the probe is 4.2 mm, and the width is 0.86 mm. The μLED (form Samsung, Inc) has dimensions of 550 μm×600 μm×200 μm. A single stimulation site is formed at the optrode tip. The working threshold of this μLED is 2.6 V, and typical forward bias voltage are 3.0 V, 3.2 V, and 3.4 V. Corresponding drive currents and power consumptions are 11.2 mA/33.6 mW, 22.6 mA/72.4 mW, and 38.2 mA/130 mW. The maximum voltage is 3.6 V, generating drive current more than 60 mA (power consumption > 216 mW). When the μLED is biased with 3.4 V, the light intensity is around 0.9 mW/mm^2; when the bias voltage is increased to 3.6 V, the light intensity would be approximately equal to 0.95 mW/mm^2. If limiting the bias voltage to 2.74 V and constraining total power to 7 mW, the local temperature increase is restricted to 0.5 °C.

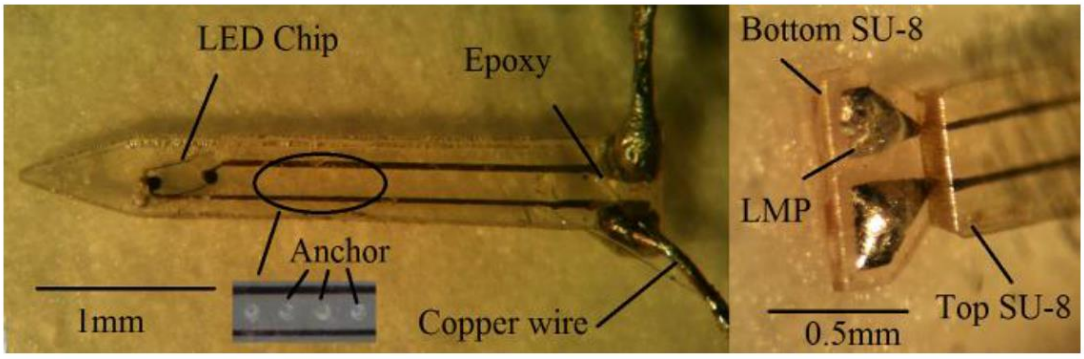


Figure 2.15 Samsung µLED mounted at the tip of the fabricated optrode [107]. Several SU-8 anchors are created along the probe shaft, enhancing the bonding strength of two SU-8 layers. Cooper wire is bonded on the probe via the low melting point (LMP). Epoxy is adopted to further strengthen the bonding robustness.

The SU-8 has outstanding flexibility, and this could decrease the tissue damage due to implantation. Also, this type of material is comparatively easy to fabricate. But, this SU-8 optrode is still with some concerns. Firstly, similar to the optrode previously mentioned (Figure 2.14), the bonded µLED is large, which is not suitable for multi-site stimulation. Secondly, the light intensity generated is not strong enough. Only when the µLED is biased with 3.6 V voltage, it could nearly meet the ChR2 activation threshold. Higher light intensity is therefore required. Moreover, the power consumption/efficiency may need to be enhanced. Given 3.4 V and 3.6 V drive voltages, power consumption levels are 130 mW and 216 mW respectively. This may not be ideal for long-term implantable applications. In addition, although the thermal increment is limited to 0.5 ℃ with an input voltage of 2.74 V, thermal effects might need to be carefully investigated when the µLED is biased with the input voltages higher than 3.0 V.

Based on this SU-8 optrode, an improved work is conducted in [108]. Instead of using SU-8, a polycrystalline diamond (PCD) substrate has been constructed to obtain an integrated optical-electrical probe, as shown in Figure 2.16. This optrode possesses two shanks. In each shank there are one µLED site and two microelectrodes, achieving optical stimulation and electrical recording. The same µLED as above (Figure 2.15) is utilised. The length of each shank is 5 mm, and the width is 1 mm. The total dimensions of this two-shank probe are 8 mm × 6.8 mm × 0.25 mm. The typical applied voltages are same to the previous work in [107], with light intensities of 0.6 mW/mm^2, 1 mW/mm^2 and 1.5 mW/mm^2. In particular, due to the excellent thermal conductivity of PCD (up to 1800 Wm^{-1}K^{-1}), this optrode

demonstrates outstanding heat dissipation performance. When the optrode is under 100 ms stimulation with 1 Hz pulses, the thermal increment is consistently below 1 °C.

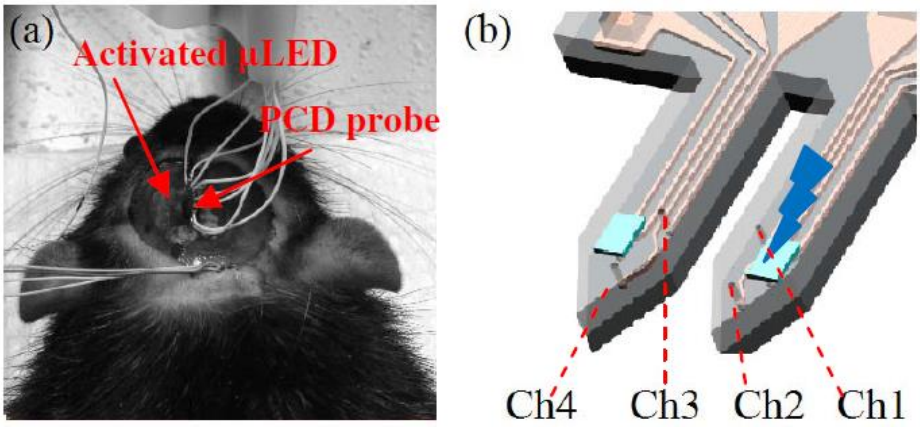


Figure 2.16 The PCD-based optical probe [108]. (a) This PCD probe is inserted into an experimental rat for the *in-vivo* test. (b) A diagram of this two-shank probe. In each shank, the μLED is placed at the shaft tip, and two recording channels are positioned in the vicinity of stimulation site.

However, although the PCD-based probe exhibits excellent thermal dissipation performance, there are still several points need to be considered. First of all, the light intensity produced is not fully sufficient for ChR2 activation. Only with a bias voltage of 3.6 V could the ChR2 threshold be triggered. A powerful light-driving ability is thus needed. Besides, the 1 mm shaft width of the probe is still over-wide, which may be likely to result in tissue injury and subsequent infection. In addition, the μLED dimensions are still a limitation for multi-site stimulation and optrode miniaturisation.

Rather than employing commercially available μLEDs, a sapphire-based optical probe with custom-designed GaN μLEDs has been developed [109], as shown in Figure 2.17. The total length of this optrode is 7 mm, with a 1mm-long shaft. The width of the optrode shaft is defined as 80 μm, to diminish the tissue damage caused by physical implantation. Five GaN μLEDs are evenly distributed along the shaft with 250 μm spacing. The diameter of each μLED is 40 μm. Six bonding pads are constructed on the optrode head. Five of these are anode pads with other a common cathode terminal. This configuration allows each μLED to be individually controlled. The maximum radiance intensity of this probe is 600 mW/mm^2, and the maximum temperature increment is limited to ~1.5 °C.

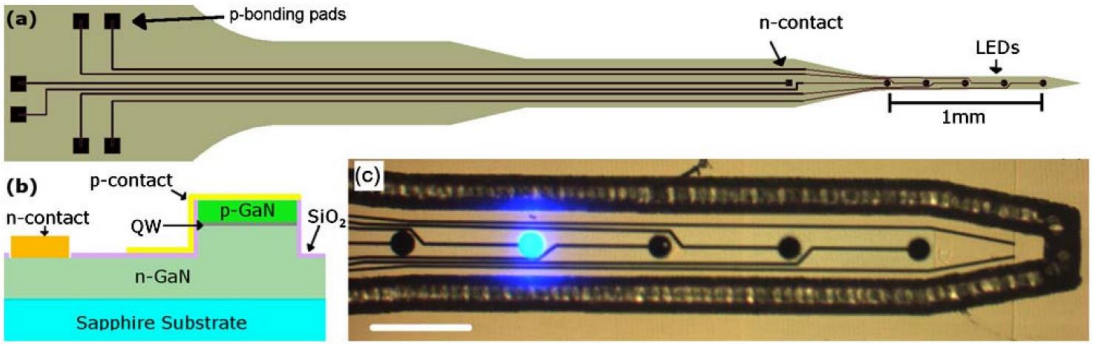


Figure 2.17 Sapphire-based GaN µLED optrode [109]. (a) System architecture of this optrode. Six bonding pads are placed at the head part to control corresponding µLEDs which are uniformly positioned along the optrode shaft. (b) The cross-section view of the fabrication process. (c) The optrode shaft including five µLEDs, one of them turned on with bright light.

This optrode accomplishes multi-site/multi-layer stimulation by applying the direct µLED-on-optrode structure. It obtains strong light intensity with a reasonable temperature increase. Nevertheless, there are still several considerations to this design. Firstly, the high material rigidity of sapphire may lead to tissue damage during or after insertion. Furthermore, the biocompatibility of both sapphire and GaN is a concern, so that further tissue infection might be caused. Besides this, due to the narrow shaft (80 µm), the future integration of neural recording electrodes would be problematic, which may prevent this device from being applied to closed-loop applications.

Based on the work illustrated in Figure 2.17, an improved work has been completed in 2016 [110]. Instead of using sapphire, silicon is utilised to construct the substrate. An image of this silicon-based neural probe is shown in Figure 2.18. This design consists of six optical shanks. Each shank includes sixteen GaN µLEDs along a 750µm-long probe shaft. By incorporating ninety-six µLEDs, this 6-shank optrode provides high-density stimulations. It demonstrates outstanding spatial resolution, and is also able to generate sufficiently strong light intensity (~400 mW/mm^2). A dedicated integrated circuit (IC) PCB is incorporated to control the probe, and each µLED can be individually addressed. Additionally, based on simulation results, with 150 mW/mm^2 luminous intensity and 50 ms operation duration, the surface temperature increases by ~ 0.5 °C on average.

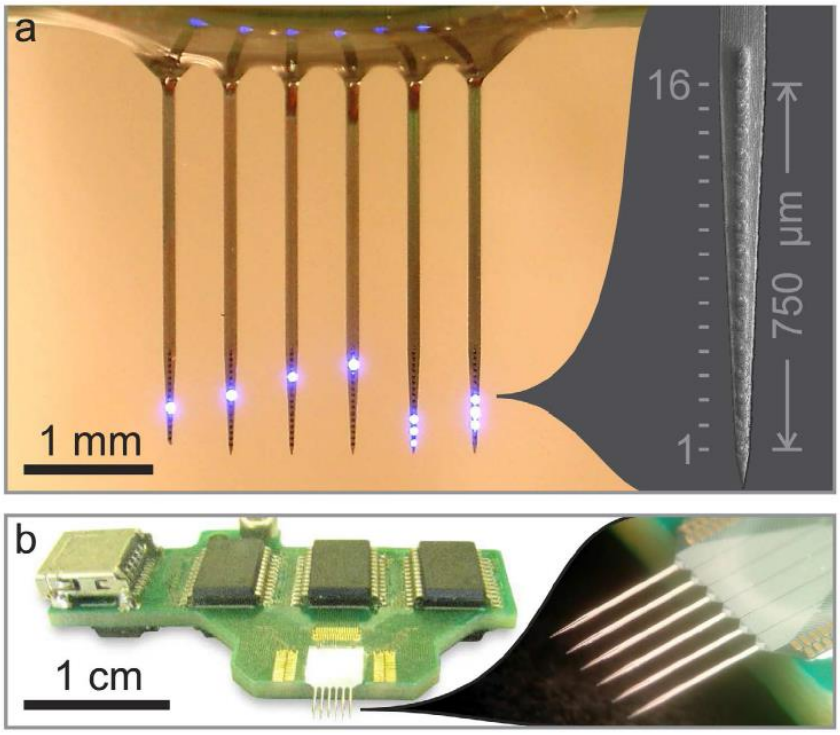


Figure 2.18 Silicon-based 6-shank GaN µLED optrode [110]. (a) 16 stimulation sites are created on each shank, and they are uniformly distributed along the 750 µm shaft. Every µLED can be individually manipulated. (b) System diagram. The fabricated optrode is bonded on a dedicated control PCB.

This brand-new optical probe has demonstrated several merits, such as high spatial resolution, strong radiance, reasonable thermal effects and the controllability/compatibility with conventional microelectronics. Even so, there are still some areas which may need to be improved. First of all, although this design demonstrates a reasonable thermal effects, these results are based only on simulation with a predefined light intensity, short operation duration and low repetition rate. It is desirable to analyse the thermal dissipation performance experimentally. In particular, even though in simulation only, the peak increment of temperature is around 4 °C. In actual use, this would be more severe if either the irradiance, working time and/or operation frequency are increased. Moreover, although the authors claims that recording electrodes could be potentially integrated into this system in the future, this might be challenging due to the narrow optrode tip and tight µLED spacing. Besides, for implantable applications, the PCB control board is relatively bulky and heavy. In addition, despite silicon being comparatively inert, biocompatibility with brain tissue may still need to be taken into account.

In contrast, a more advanced multifunctional injectable probe has been created based on flexible microelectronics [111], as illustrated in Figure 2.19. This design transforms the conventional solid optrode substrate into a flexible polymer base. Moreover, it integrates different material layers to achieve multiple functions, including electrical recording (Layer 1), optical detection (Layer 2), optical stimulation (Layer 3), and thermal sensing (Layer 4). In particular, a releasable base is built into this probe. During implantation, this injectable μneedle leads all of the functional layers into the targeted tissue region. After insertion, the μneedle is removed using dissolving fluid, and only the functional components are kept in the subject brain. The total thickness of all injected layers is only ~ 20 μm, which will greatly minimise any tissue damage induced by device insertion. The maximum light intensity is ~40 mW/mm^2, which is sufficient for opsins activation. If the light intensity is limited to 17.7 mW/mm^2, the temperature increase is restricted to 1 °C. Additionally, this device is compatible with wireless power transmitter, which could be highly beneficial for the freely-moving animal experiments.

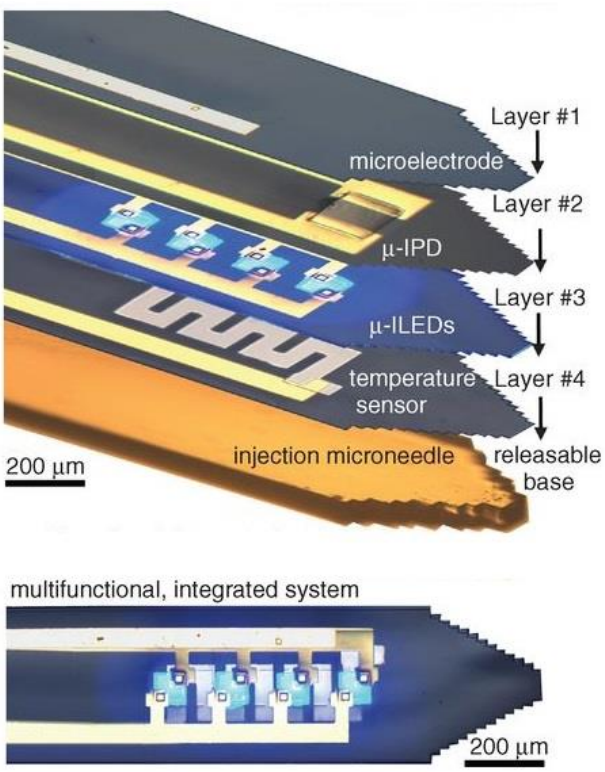


Figure 2.19 Flexible electronics-based multifunctional implantable probe [111]. Four different functional layers are incorporated along with a releasable base. The recording microelectrode is constructed on Layer 1; and then a micro-inorganic photodetector (μIPD) is utilised for photodetection at Layer 2; Layer 3 contains four micro-inorganic LEDs (μ-ILEDs) for optogenetic stimulation; and Layer 4 is dedicated to temperature sensing.

This multifunctional implantable probe combines an optogenetic stimulator, recording electrode, photo detector, and temperature sensor in an integral device. It demonstrates excellent properties compared to the other devices reviewed above. Nonetheless, several concerns have been still identified and may need to be addressed in the future. One concern is the system thermal effect. The overall temperature increase can be limited to 1 ℃, but this is on the condition of 17.7-mW/mm^2 radiance. Given continuous 23.5 mW/mm^2 light power, the temperature rise would reach 10 ℃. Also, these thermal analysis results are obtained on the condition that the device is only implanted at a depth of 0.3 mm into the brain of the subject. The thermal increment would be higher with further insertion. Both the above situations may potentially cause thermal damage to the brain tissue. Another concern is its relatively low light intensity. This device is able to achieve a maximum light intensity of 40 mW/mm^2. Although this value is much higher than the ChR2 activation threshold, it may not be sufficient for high-intensity deep-penetration applications. Moreover, under wireless control mode, only 7 mW/mm^2 radiance is generated using 4.08 mW input electrical power. This indicates that the power efficiency still has some room for enhancement. Furthermore, the total length of the probe shaft is less than 1 mm, and this would become problematic for neural stimulation in deeper cortex areas. Besides, the construction of this multifunctional optrode relies on a costly and complicated custom-fabrication flow, which may result in restrictions for other researchers' adoption. In addition, due to the system complexity, utilising a conventional microelectronic device to conduct logic control and two-way communication with the implant might be another challenge. Finally, operational degradation, such as electronic failure or mechanical breakage, might also need to be carefully considered.

Based on the literature survey conducted above, a performance summary of recently published μLED-on-optrode structure based optogenetic implants is presented in Table 2.2. Recent advances in μLED-on-optrode devices provide the feasibility to directly interact with deep brain tissues via optrodes. However, although these devices can achieve direct light delivery for optogenetic stimulation, their performances could still be enhanced from different aspects. Some devices could only obtain relatively weak light emission, which would be challenging for ChR2 (or other opsins) activations. Some devices can generate sufficient luminance,

but they lack appropriate intensity modulation methods. Moreover, a very critical concern for implantable applications is safety. In particular, substrate integrity and operational degradation of light emitters are two dominant factors, which need to be taken into consideration. Besides, thermal dissipation is always a major concern for μLED-on-optrode structure. It is vital for both system stability and tissue health. Suitable thermal management is demanded, and temperature sensing circuitry is required to be integrated into the implant. Furthermore, electrical neural recording circuitry is desirable to be imported into the optogenetic implants, realising closed-loop integration. Some optical implants have incorporated recording electronics, but they use separate fabrication processes and/or control electronics from those used for the optical stimulators. This might increase the design and fabrication complexities, and cause difficulties for system integration. In addition, most of the current devices have been custom-fabricated. This might require comparatively huge financial and labour resources, and, more importantly, restrict their broader adoptions. Most importantly, all of these devices are controlled by external instruments/electronic systems. There are no active implantable electronics built inside to internally control the implants. All functions such as optical stimulation, electrical recording, and thermal sensing are performed via passive drive/control electronics. This may lead to a heavyweight for the overall system, and add obstacles for freely-moving animal experiments and clinical trials. Besides, their external control electronics are mostly not fully compatible with conventional biomedical microprocessors, which might limit their widespread applications.

Table 2.2 Performance summary of recently published µLED-on-optrode structure based optogenetic implants.

Ref.	Dimensions	No. of Sti Sites	Max Light Intensity	Max Power	Control Electronics	Integrity / Degradation Evaluation	Thermal Increment	Thermal Sensing	Electrical Recording	Substrate Material
[105]	Shaft: 12 mm; Width:900 µm; µLED: 1000 × 600 × 200 μm^3	1	0.7 mW/mm^2	Power: 14.5 mW	External instruments	No	N/A	No	Yes	Polyimide
[107]	Total length: 4.2 mm; Width: 0.86 mm; µLED: 550 × 600 × 200 μm^3	1	0.95 mW/mm^2	Power: > 216 mW	N/A	No	0.5 °C increase with 7 mW power & 2.74 V input voltage	No	No	SU-8
[108]	Shank Length: 5 mm; Width: 1 mm; µLED: 550 × 600 × 200 μm^3	1	1.5 mW/mm^2	Voltage : 3.6 V	External instruments	No	1 °C increase with 3.6 V input voltage	No	Yes	Polycrystal line Diamond
[109]	Total length: 7 mm; Shaft: 1 mm; Width: 80 µm µLED: 40 µm diameter	5	600 mW/mm^2	N/A	External instruments	No	1.5 °C increase with 600 mW/mm^2 and 200 ms pulse	No	No	Sapphire
[110]	Total length: 3 mm; Shaft: 750 µm; µLED: 25 µm diameter	16	400 mW/mm^2	Current: 5 mA	External PCB control boards	No	0.5 °C increase with 150 mW/mm^2 radiance and 50 ms pulse; Maximum: 4°C	No	No	Silicon
[111]	Shaft: 1 mm; Width: ~ 400 µm; Thickness: ~ 20 µm; µLED dimensions: 50 µm × 50 μm^2	4	~ 40 mW/mm^2	Power: 40 mW	External flexible/rigid control boards	No	1.0 °C with 17.7 mW/mm^2 radiance and 10 ms pulse; Maximum: 10°C	Yes	Yes	Platinum, Silicon, Polymer

2.4.4 Summary

This section has reviewed recently published work on optogenetic implants. Wave-guiding structure and μLED-on-optrode structure have both been investigated. The limitations of each reviewed device have also been identified. Following this, several observations are presented below.

Light Delivery Stability and Precision

For implantable optical stimulation, stable light delivery is demanded. Laser sources provide coherent light emission with low divergence, and μLEDs achieve more stable light delivery. One concern of the wave-guiding structure is its low coupling efficiency with both lasers and LEDs. Another concern is that, due to their bulky dimensions, the multiplexing of wave-guiding structures for multi-site stimulation is challenging.

Optrode Dimensions

The optrode dimensions must be miniature. Several of the existing devices are comparatively large which may not be suitable for implantable animal experiments. The length of optrode shaft should be around 4 mm, achieving implant miniaturisation and matching the cortex thickness [106]. The shafts of some of the optical probes reviewed above are relatively short (around 1 mm or even shorter), which would make them unusable for deeper multi-layer stimulation. Optrode width and thickness (or diameter) should be within micrometre scale, minimising the potential tissue damage caused by device insertions. The head part of the implant should be of small dimensions and light weight. The probe heads of several existing devices occupy large spaces, which may cause an extra burden for experimental subjects. Also, light emitters should be designed with minimal dimensions. This will help to increase luminance intensity, and facilitate multi-site stimulation, and also further minimise the implant.

Spatial Resolution and Temporal Resolution

The implant should be applicable to extensive brain network to allow the analysis of complex neural circuitry. It should hold appropriate spatial resolution (in the micrometre scale) for multi-site and multi-layer stimulation. Besides this, although

the pulse frequency of stimulation operation is fairly low (typically less than 1 kHz), it is desirable to realise relatively high temporal resolution so as to improve the stimulation accuracy and efficiency.

Intensity Controllability

Light intensity controlling presently relies on manually changing the stimulation pulse width and/or shifting the driving current/voltage. It is desired and important to incorporate a more advanced control mechanism so as to achieve finer overall intensity modulation. This would be meaningful for optimising light/power efficiency, enhancing stimulation precision, improving operational safety, and regulating temperature increases. Additionally, high-intensity emission is required, especially for deeper penetration applications.

Intelligent Implantable Electronics

To date, all of the existing optogenetic implants are passively controlled by different external controlling devices. This might increase the development complexity of the implantable system. Different implants require diverse dedicated controlling equipment, which might be cost-ineffective and labour-intensive. More importantly, these external controlling devices are not entirely compatible with those implants developed by other researchers. This would limit their broader applications. Besides, the relatively bulky dimensions and high power consumption of these controlling systems may further restrict the adoption of the implants in freely-moving animal experiments and/or clinical applications. Thus, there is an increasing need to construct an intelligent optogenetic implant for actual medical utilisations. Active controlling electronics should be built inside the implant, which should be able to actively perform all required operations as a smart system. Standard communication protocol (such as Serial Peripheral Interface, SPI) should be embedded into the device, and moreover, this active implant should be compatible with general biomedical microcontrollers, so as to be easily adopted by the wider research communities and society.

Integrity and Degradation Evaluation

As the implant would be inserted into the brain, it will be difficult for clinical staffs/patients to observe its real-time working status. In particular, any breakage or

component failure occurring in the implant may lead to high risks to patients' health. None of the studies published so far include a relevant evaluation strategy created within the implants. Thus, it would be advantageous to incorporate a dedicated sensing scheme for the evaluation of the system integrity and long-term durability.

Thermal Effect

Heat dissipation is of crucial importance in any optical implant, especially for the μLED-on-optrode structure. However, only a few existing devices take the thermal management into account. Detailed thermal analyses is essential to be conducted for proposed optrodes, and it is necessary to restrict temperature increases by a reasonable boundary (ideally within 2 °C [112-114]). Moreover, it is desirable for temperature sensors to be incorporated, which can monitor the system thermal effects in real-time. This will benefit both system stability and tissue health.

Neural Recording Function

The use of a closed-loop neural interface is a growing trend in neuroprosthesis applications. The majority of current optogenetic implants are still conventional open-loop systems. For a new type of optogenetic implants, neural recording components should be built in. Local neural activities could then be observed to provide in-situ feedback signals for stimulation operation. This could improve the system functioning performance, operational efficiency, and power efficiency.

Fabrication Technology

Most existing optogenetic implants are custom-fabricated, which might be comparatively costly and labour-intensive. This may also create a barrier for widespread adoption and application. Thus, it is demanding to construct optogenetic implants using a commercially available fabrication process.

Power Consumption

Power consumption is also important for implantable applications, and it is critical for both battery operation and wireless power transmission. Most existing devices require strong current/high voltage, or their designs have not taken the power budget into consideration. It could be meaningful to optimise the system power consumption.

To conclude, various fabrication technologies have been investigated and utilised for the development of optogenetic implants. Although these existing devices can meet the need of optogenetic stimulation to some extent, they have some areas for enhancement, in terms of illuminance stability, multi-site operation, intensity controllability, and miniaturisation. Moreover, it is desirable to incorporate different sensing and evaluation schemes into the implant. This could highly improve the overall system performance, with regard to safety, reliability, operation efficiency and functioning accuracy. Thermal sensing components, neural recording electronics, and integrity & functioning evaluation schemes should be built into the implant. More importantly, the targeted implant should be actively driven, acting as an intelligent standalone system. This intelligent implant should be fully compatible with conventional biomedical microprocessors, which can be widely unitised in the broader biomedical engineering field. In addition, the targeted implantable device is expected to be fabricated using a commercially available technology, which would be more convenient for other researchers to adopt.

2.5 Conclusion

In this chapter, the basic concepts of neuroprosthetics have firstly been introduced in Section 2.2. Typical neuroprosthetic applications have also been illustrated. At the cutting-edge of engineering and science, it can be seen that the neuroprosthetics field is already and will continuously impact the broader society. In Section 2.3, the emerging optogenetic technology is briefed with basic principles and selected applications. This technology constructs a new path to address common brain illnesses and neurological disorders. Due to the outstanding features held by optogenetics, there is a strong need to develop advanced optogenetic implants for stable local light delivery and multi-site stimulation. Then Section 2.4 has reviewed recently published work in this area. Different development strategies for optogenetic implants have been investigated, and their limitations have also been pointed out. In particular, primary development criteria of the new type of optogenetic implants have been summarised in Subsection 2.4.4. These criteria provide a baseline for the design specifications of the targeted implant, as detailed in Chapter 3.

3 Design Concept and Specifications

3.1 Introduction

The last chapter has reviewed recently published studies on optogenetic implants using different fabrication technologies. Their strengths have been highlighted and their weaknesses have also been identified. The development criteria for the targeted optogenetic implant have then been deduced, and these provide the key design specifications for the proposed optrode.

In this chapter, a CMOS-driven GaN μLED approach is proposed to develop a new type of optogenetic implant. This design aims to provide effective optogenetic therapies for neurological and psychiatric illnesses, such as epilepsy, Parkinson's disease and blindness. Multi-site light delivery needs to be achieved in a single optrode. In particular, in-built diagnostic sensing circuitry could be constructed to evaluate the system integrity and light emitter degradation. This strategy can largely enhance optrode safety and reliability post-implantation and during long-term normal operation. Furthermore, in-situ temperature sensors should be incorporated to investigate the thermal effect of the implant, and this would be advantageous for both tissue safety and device stability. Moreover, electrical neural recording circuitry could be integrated into the implant so as to observe local neural signals in the vicinity of each optical stimulation site, accomplishing an advanced closed-loop neuroprosthetic system.

In the following sections, the conceptual design of the optrode is firstly introduced; then the design criteria and specifications are elaborated from different perspectives, including intelligent implantable electronics, fabrication technology, multi-site optical stimulation, self-diagnostic function, thermal analysis and sensing, electrical neural recording, and power budget.

3.2 Conceptual Design

Figure 3.1 demonstrates a conceptual diagram of the proposed neural optoelectrode design, which is based on the μLED-on-optrode structure. Recording

microelectrodes are spaced across the cortex to observe local neural activities, providing real-time feedback neural signals for the optical stimulator. Then the optical stimulator can determine whether to activate specific μLEDs to deliver light into brain tissue, modulating those optogenetic-targeted neurons. This feedback scheme also helps clinical staffs/patients to define the light intensity and stimulation cycle. This closed-loop system is controlled via a general chest biomedical microcontroller. In-built fraction sensors (diagnostic sensing circuitry) and thermal sensors are created to evaluate the system integrity and monitor the heat effect. This would ensure both circuitry stability and tissue health.

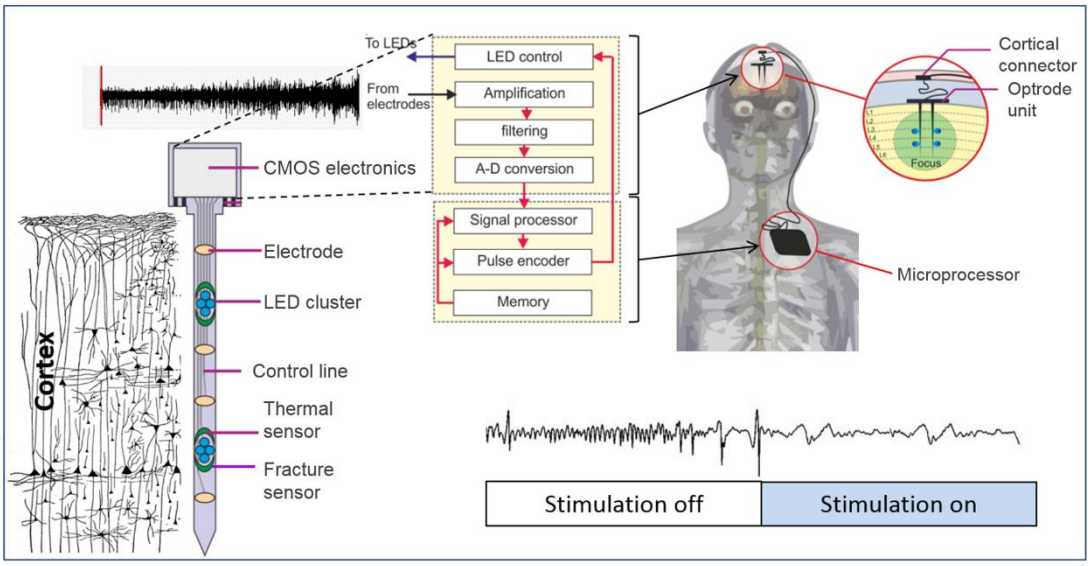


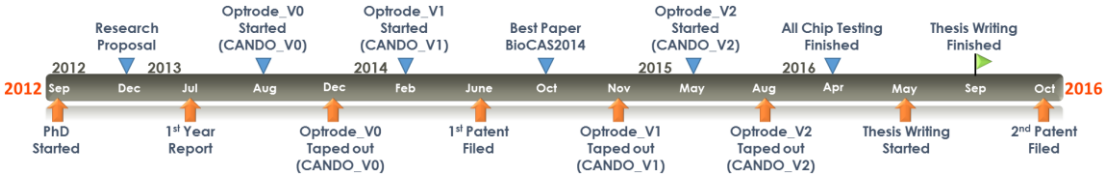
Figure 3.1 Conceptual diagram of the proposed optrode. This multifunctional optogenetic implant is fabricated in standard CMOS process. It mainly consists of optical stimulation circuitry, electrical recording circuitry, diagnostic sensing circuitry, and temperature sensing circuitry. The optrode can be utilised in practice with general neuroprosthetic pacemakers. Closed-loop algorithm would be embedded into the biomedical processor. This figure is modified from [115].

3.2.1 Potential Applications

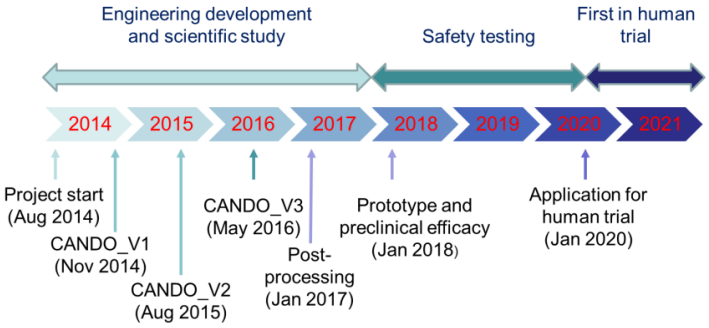
Epilepsy - CANDO Project

A very useful application of the proposed optrode is epilepsy. As a typical neurological disorder, epilepsy has currently affected more than 600,000 people in the UK [77], which devastates the quality of patients' life. In August 2014, a seven-year £10M biomedical project, called Controlling Abnormal Network Dynamics using Optogenetics (CANDO, www.cando.ac.uk), is launched, and this project aims to create the first clinical trial of the optogenetic implant in epileptic

patients. My PhD work mainly contributes to this project. Figure 3.2 shows the timing lines my PhD and CANDO project, respectively.



(a)



(b)

Figure 3.2 (a) My PhD timing line, from September, 2012 to September 2016. (b) CANDO project timing line, launched August, 2014.

Visual Prosthesis

Another promising application of this optrode is blindness. Figure 3.3 shows a general diagram of an implantable visual cortical prosthesis system using the optrode. Front camera would be used to receive outside imaging signals and send them to a biomedical processor on the glasses. Then the biomedical processor could control the optrode to stimulate the targeted visual cortex neurons to restore the visual sense. A wireless power & data transfer system will be developed for the implantable system. This project would be fully explored and developed in the future.

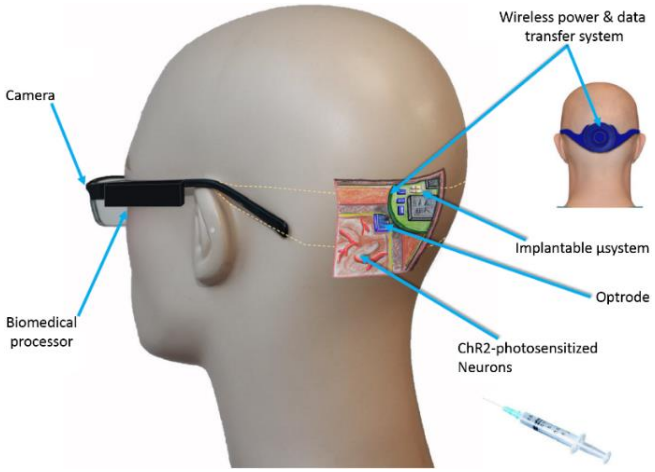


Figure 3.3 General diagram of an implantable μsystem for visual cortical prosthesis [116]. It mainly consists of a front camera, a biomedical processor, an optrode array, and a wireless power & data transfer system.

Other potential applications of the proposed optrode, such as Parkinson's disease, dystonia, tremor, and tinnitus, are not depicted here.

3.2.2 System Architecture

Since the proposed optogenetic implant is targeted to be applied into the cerebral cortex, the proposed implants should fit with the natural structure of cerebral cortex. A histological structure of the cerebral cortex is illustrated in Figure 3.4. It mainly consists of six layers. The overall average thickness of the cortex is 2.5 mm, typically varying between 2 mm and 4 mm [106]. Therefore, multiple stimulation sites should be developed for six-layer stimulation. An appropriate shaft length should be defined to suit the cortex thickness. As this is variable in the 2 - 4 mm range, the shaft length can be defined as 4 mm to cover all the patients' needs. In order to minimise the damage caused by device insertion, the shaft width should be narrow. On the other hand, with a view to guaranteeing system robustness, the shaft width cannot be over thin. Based on the literature survey in Chapter 2, the typical shaft width of the μLED-on-optrode structure varies from 80 μm to 1000 μm. After discussing with mechanical engineers and fabrication specialists, in order to achieve a trade-off between tissue damage and shaft durability, the shaft width should be in the 200-300 μm range. This width can also accommodate local circuits wiring in the system integration stage. In addition, the optrode head should be of reasonable dimensions and weight, so as to be convenient for *in-vivo* tests.

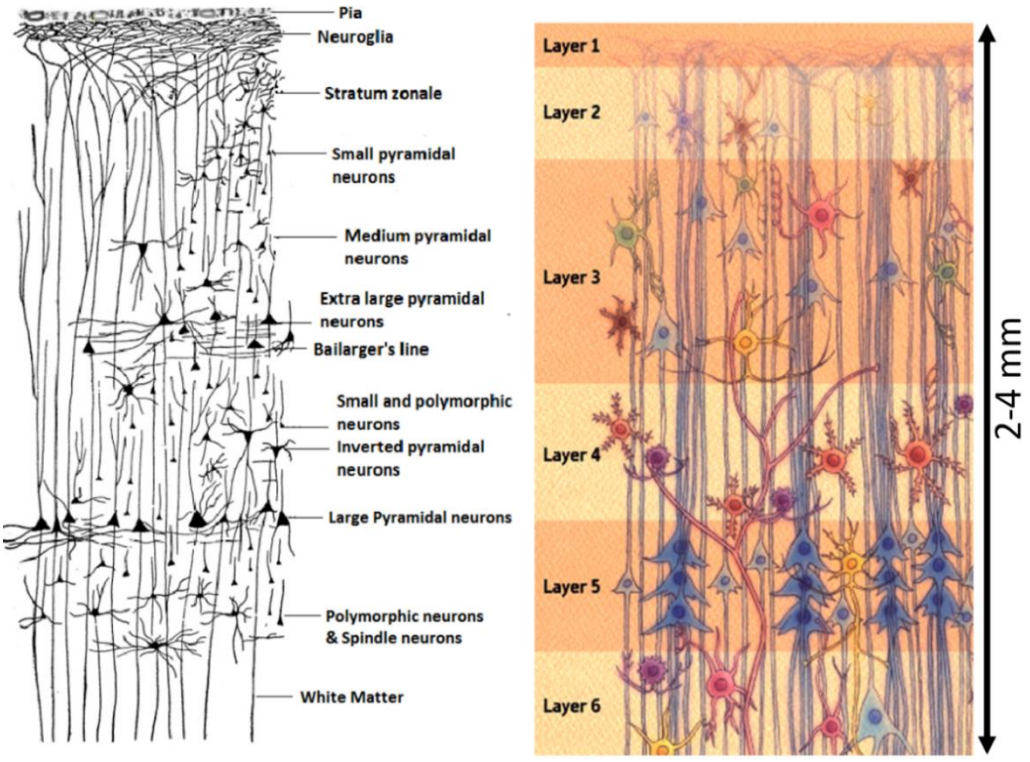


Figure 3.4 Histological structure of the cerebral cortex [117]. The cortex includes six layers, and the thickness of cortex layers varies from 2 mm to 4 mm with an average value of 2.5 mm.

The general design floorplan is displayed in Figure 3.5. The dimensions of this optrode are scalable. The optrode shaft length is set as up to 4 mm, matching cortex thickness. In order to fit all the controlling electronics into the implant, the optrode head should has an appropriate dimension. Based on the area estimation of main circuits, the maximum dimension of optrode head is defined as 1 mm × 2 mm for the first instance. This also ensures the light weight and small size of the headstage. The width of the optrode shaft is up to 300 µm, so as to minimise tissue damages induced by implant insertion. This proposed optrode is fabricated in a commercially available CMOS process. All the electronics are developed using conventional microelectronics technology, to realise the stimulation, recording and sensing circuitries. Optical stimulation sites and electrical recording sites are both constructed along the optrode shaft, achieving multi-layer optical stimulation and in-situ multi-channel electrical recording. For each stimulation site, three (or more) µLEDs are built as a µLED cluster. One of the µLEDs is set as the main emitter, and the other act as backup components. If the main emitter is faulty, an alternate µLED will then be switched on. This backup mechanism improves system robustness and long-term durability. By applying this cluster setting, adjustable-area and adaptable-depth stimulation are also achieved, enhancing the stimulation spatial resolution.

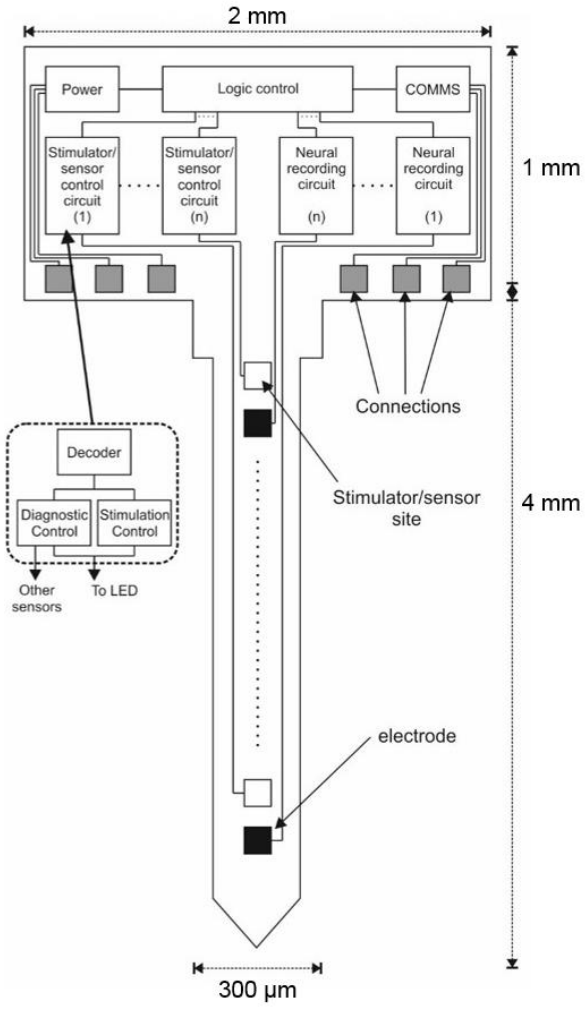


Figure 3.5 General design floorplan of proposed optogenetic implant. The (max) dimensions of the implant are 2 mm × 5 mm, and the (max) size of the optrode shaft is 300 µm × 4 mm. A logic control and communication block is placed at the top of the optrode head. It determines all the input & output data for the stimulation, sensing, and recording circuitry.

The proposed optrode aims to be utilised for distributed targets in 3D brain network. Thus, individual control block is developed for each stimulation site, in which contains one stimulation control block and one sensing block (diagnostic sensing and/or thermal sensing). This guarantees that every µLED/sensor can be manipulated independently for dispersed targets. Similarly, every recording point is accessed by a dedicated recording control block. All these individual control blocks (both stimulation and recording) are positioned at the optrode head. However, in actual implementation, these control blocks can also be placed along the optrode shaft, in the vicinity of each stimulation/recording site. This can further minimise the device dimension and improve system operation accuracy. Different physical configurations are described in Chapter 5.

3.3 Intelligent Implantable Electronics

Currently, all the existing implants are passively controlled by specific external controlling systems, which add development complexities. This might also increase the resources cost. Moreover, most of these dedicated controlling devices are not compatible with other optrode designs, which may restrict their broader utilisations. Furthermore, some controlling instruments hold comparatively high power consumption and large dimensions, which may further constrain the natural behaviour of experimental subjects. Therefore, there is a growing need for engineers to construct an intelligent optical implant in which all operations can be actively performed. Such an active optogenetic implant should act as a smart system and be fully compatible with general biomedical processors. In this stage, standard communication protocols, like SPI bus, can be embedded into the system for logic control and two-way communication. As demonstrated in Figure 3.5, central logic and communication modules are created inside of the optrode to manage all the input and output signals. In the future, the DC SPI protocol can be replaced by Alternating Current (AC) based CANopen (Controller Area Network) protocol, which are more compatible for chronical human use.

3.4 Fabrication Technology

The selection of fabrication technology is another concern in implant implementation. It can be observed from Chapter 2 that existing optogenetic implants have been all implemented using customised fabrication processes, which are cost-ineffective and labour-intensive. Moreover, most of these fabrication techniques are comparatively complicated. This causes difficulties for other researchers to adopt them for wider applications.

In the optical implant proposed in this thesis, commercially available CMOS process is selected for manufacture. As a mature semiconductor fabrication technology, the CMOS process is more cost-efficient and easily adaptable for other researchers' use. In general, optical implants require comparatively high voltages ($\geq$ 5 V, details are described in Section 3.5) to drive the blue light emitters. Thus the maximum operation voltage to be supported is one important factor in defining the optimal CMOS process (which supports a 5 V operation voltage). The feature size of

the process is another factor in technology selection, as it is key in defining implant miniaturisation. The integrating density also affects optrode dimensions to some extent (determining the area of digital cells). Moreover, price is another consideration. A comparison of different CMOS processes available for fabrication is summarised in Table 3.1.

Table 3.1 Technology comparison of typical CMOS processes.

	AMS C35	AMS H35	AMS C18	XFAB XH035	XFAB XH018
Core Voltage (V)	3.3	3.3	1.8	3.3	1.8
Max Operation Voltage (V)	5	50	5	5 (100)	21
Feature Size (um)	0.35	0.35	0.18	0.35	0.18
Integrating Density (k gates/mm^2)	18	18	118	28	125
Price (€/mm^2)	580	900	1050	-	1430

Based on the criteria identified above, the AMS C35B4C3 technology is selected for device fabrication. This technology can provide 5 V voltage for light emitters. It also has a reasonable price for fabrication. Although its integrating density is relatively low, it is sufficient for the proposed optrode design. If needed, it could be switched to AMS C18 technology to further minimise the implant. In particular, the first version optrode (in Chapter 5, Section 5.2) is fabricated in XFAB XH035 process, being combined with other designs from our lab.

Additionally, the fabricated optrodes will be directly cut-out as an integral T-shape from the CMOS dies or wafers. This fabrication strategy can simplify the post-processing of the device.

3.5 Multi-site Optical Stimulation

For optogenetic stimulation, stable and precise light delivery is an essential requirement. Besides, multiple stimulation sites are required on a single optical probe, which can then be applied in a large brain network. To accomplish targeted optical stimulation, the selection of an appropriate light source is necessary. Among all existing optogenetic implants, lasers (or laser diodes) and LEDs are utilised, both of which have different merits and limitations.

Fibre-coupled laser structures are able to generate high-powered light emissions. The light power could be up to 100 mW or even more. Another merit of laser sources is their relatively low beam divergence. This guarantees direct photo-stimulation to the brain area of interest. However, laser-based structures also have some limitations such as long warm-up time, high cost, high power consumption and fluctuations [92-94]. Moreover, due to the bulky size of optical fibres, it is very challenging for the solitary fibre-coupled laser source to be multiplexed for multi-site stimulation, with individual control of each stimulation site. In contrast, LEDs hold more flexibilities for optogenetic experiments. Multiple μLEDs can be directly bonded onto the optical probes, and then inserted into the brain to achieve multi-site local light emission. In a single LED-based optical probe, μLEDs can be individually accessed and controlled. Thus, μLEDs are more suitable for the construction of multi-site optogenetic implant.

In the following subsections, the fundamentals of LEDs are briefed; then different design requirements for the targeted photostimulation are elaborated.

3.5.1 Fundamentals of LEDs

A LED is an electroluminescence-based electronic light source [118-120]. Electroluminescence is an optical-electro phenomenon, which converts an electronic input into a light output. The core part of the LED structure is the *p*-*n* junction. A LED can be considered as a specific *p*-*n* junction diode which could achieve optimised electroluminescence [118]. The LED can emit light in different modalities: ultraviolet, visible and infrared. For optogenetic stimulation, light sources are working in the visible region.

Typically, a LED has three distinct operation states, of which Forward Bias is the commonly used. A typical working flow of the LED under forward biased is illustrated in Figure 3.6. When the LED is configured to the forward biased state, holes and electrons are respectively injected from the *p*-side and the *n*-side. As the applied voltage V_F is higher than the intrinsic built-in potential of the *p*-*n* junction, these carriers can pass across the junction. They then become excess minority carriers, and subsequently recombine with the majority carriers. The band-to-band recombination happens mostly in the junction, and a photon is then formed in which the energy hv is equal to the band gap, E_g. The wavelength of produced light λ is also defined.

$$hv = E_g \tag{3.1}$$

$$\lambda = \frac{1.24}{hv(eV)}\ \mu m \tag{3.2}$$

Where hv is the energy of the emitted photon, E_g is the energy gap.

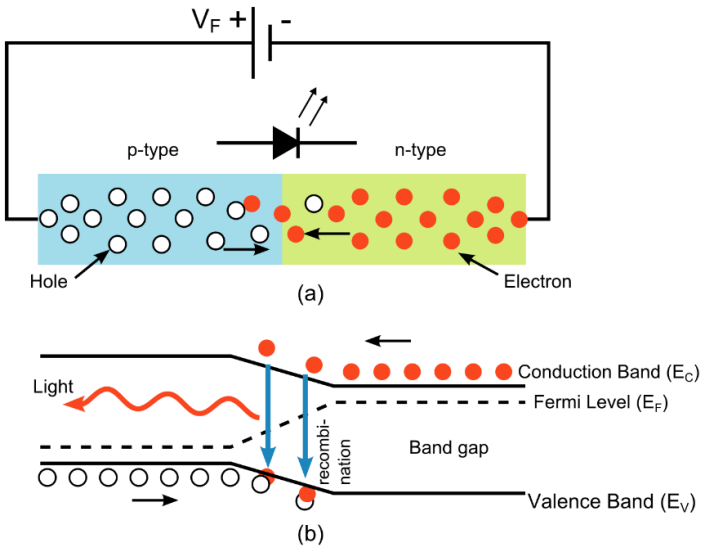


Figure 3.6 LED forward bias state. (a) V_F is applied to forward bias the LED, and holes are flowing from the *p*-side and electrons are injected from *n*-side. (b) When an electron meets with a hole in the vicinity of the junction, the recombination occurs, and energy is released in the form of a photon. The figure is modified from [120].

The other two LED operation states are Reverse Bias and Breakdown. In the reverse bias state, a negative voltage difference exists across the LED terminals, and a negative leakage current passes through the LED. If further increasing the negative voltage, the LED enters the Breakdown operation region and a strong negative breakdown current is then be generated. A typical LED *I-V* characteristic relationship is displayed in Figure 3.7. The corresponding equation expression of the LED is also illustrated below.

$$I_0 = K_0\, e^{\frac{-qV_0}{nkT}} \tag{3.3}$$

$$I = I_0\,(e^{\frac{qV}{nkT}} - 1) \tag{3.4}$$

Where I_0 is the reverse saturation current, I is the current through the LED, q is the charge of an electron, K_0 is a *pn* junction-geometry depended constant, V_0 is the built-in voltage, k is the Bolzmann's constant, T is the absolute temperature, and n is the ideality factor (a geometry-based factor, usually in 2-3 range [118-119]).

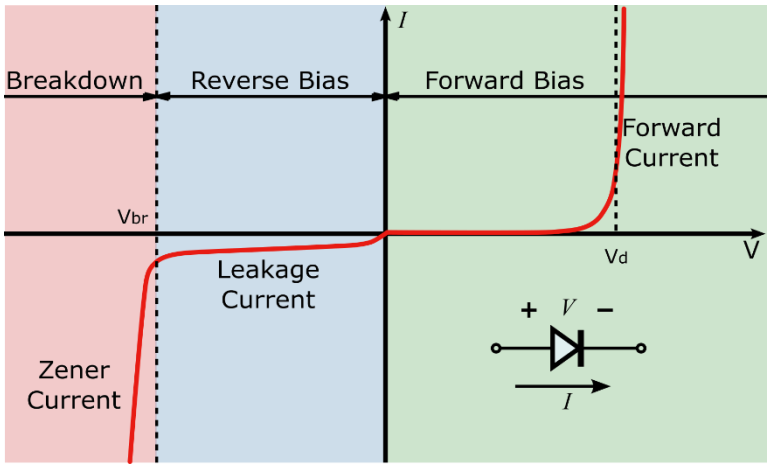


Figure 3.7 Different operational states of the LED: Forward Bias, Reverse Bias and Breakdown. V_d is the threshold of the LED under forward bias, and the V_{br} is the breakdown threshold.

A LED is a monochromatic component, and it emits pure colour light in a narrow spectral range. Table 3.2 summarises the relationship among colour, wavelength and typical materials of LEDs. In optogenetic applications, blue light with a wavelength of 470 nm is widely chosen for ChR2-based photo-stimulation [57, 89].

Table 3.2 Relationship between common LED colours, emitted wavelengths, and typical materials.

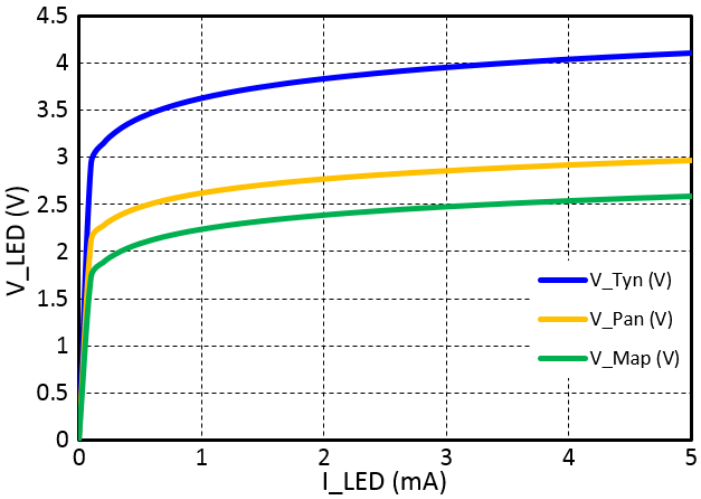
Colour	Infrared	Red	Orange	Yellow	Green	Blue	Violet	Ultraviolet
Wavelength (nm)	$\lambda > 760$	$610 < \lambda < 760$	$590 < \lambda < 610$	$570 < \lambda < 590$	$500 < \lambda < 570$	$450 < \lambda < 500$	$400 < \lambda < 450$	$\lambda < 400$
Material	Gallium arsenide (GaAs)		Aluminium gallium phosphide (AlGaP)		GaN			Diamond, Boron nitride

For the proposed optogenetic implant, custom-designed blue µLEDs with a diameter of 20 µm will be utilised as light emitters. These µLEDs will be provided by Tyndall National Institute, Ireland (which are currently under development). In the meantime, other two types of LEDs are also adopted for on-bench electrical validations (from Panasonic Corporation and Maplin Electronics respectively). The main parameters of these three types of LEDs are listed in Table 3.3.

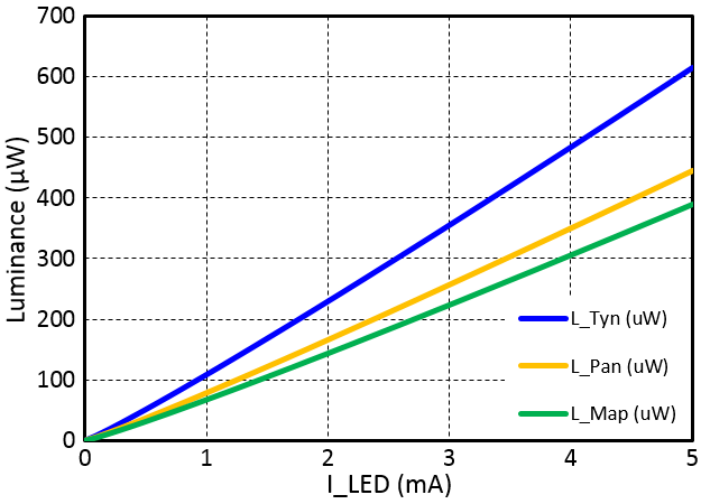
Table 3.3 Main parameters of three different types of 470-nm LEDs.

LED Type	**Forward Current (Typ) (mA)**	**Forward Voltage (Typ) (V)**	**Forward Current (Max) (mA)**	**Forward Voltage (Max) (V)**	**Diameter**
Tyndall	1	3.65	10	4.32	20 µm
Panasonic	5	2.97	40	3.9	200 µm
Maplin	25	3.2	100	4.07	5 mm

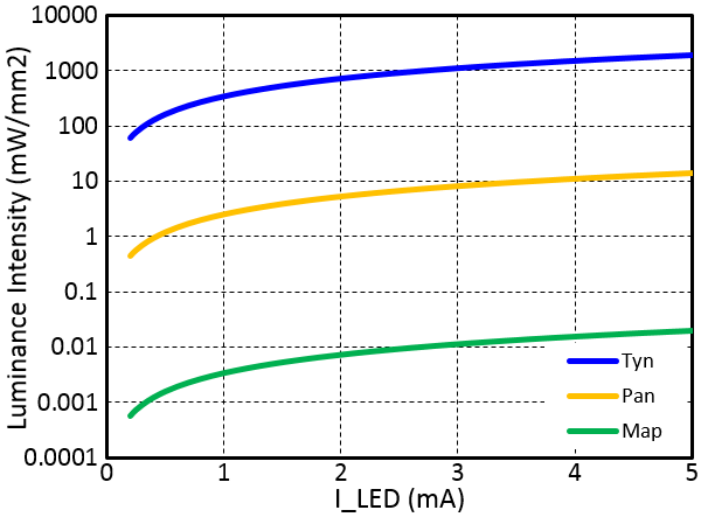
In order to characterise the *I-V* and *I-L* (*Luminance*) relationships, corresponding electrical and optical measurements of a solitary Tyndall µLED has been conducted. Moreover, similar measurements have been performed to characterise the *I-V-L* features of the Panasonic and Maplin LEDs. The *I-V-L* feature curves are then displayed in Figure 3.8, and the main parameters are summarised in Table 3.4. It can be observed that although these three LEDs have similar luminance levels, their light intensities are significantly different. This is because of their distinct dimensions. Smaller dimensions can provide higher intensity, and vice versa. Therefore, the Panasonic and Maplin LEDs are only used for performance validation purposes. For practical use, miniature Tyndall µLED will be bonded once it is provided from the vendor, and the bonding processes will be developed by the fabrication team at Newcastle University. The small-size µLED can also benefit multi-site configuration and local circuitry integration. But, as the Tyndall µLED will be not in place before the completion of my PhD, in this thesis, all the experimental data are collected from the Panasonic µLEDs. This is because the Panasonic µLED has closer luminance driving ability with Tyndall µLED. And all the simulation results are obtained from a Verilog-A based Panasonic µLED model which is deduced based on the experimental *I-V-L* features below.



(a)



(b)



(c)

Figure 3.8 *I-V-L* relationships of three different types of LEDs. The current through each LED is steadily increased from 0 mA to 5 mA. (a) *I-V* relationship. (b) *I-L* relationship. (c) *I-Luminance Intensity* relationship.

Table 3.4 *I-V-L* parameters of three different types of LEDs.

LED Type	**Input Current (mA)**	**Voltage (V)**	**Luminance (µW)**	**Luminance Intensity (mW/mm^2)**
Tyndall	0 - 5	0 - 4.1	0 - 615	1959.6
Panasonic	0 - 5	0 - 2.97	0 - 445	14.18
Maplin	0 - 5	0 - 2.63	0 - 389	0.0198

3.5.2 Luminance Driving Ability and Controllability

Luminance Driving Ability

Light intensity is a major factor in optical neural stimulation. It not only determines whether the implant can activate a specific opsin, but also defines the penetration depth of brain tissue. As mentioned above, for ChR2-based optogenetic stimulation, the activation threshold is around 1 mW/mm^2. This requires the selected µLED to provide sufficient radiant intensity to trigger the ChR2 opsin. Moreover, for targeted tissue penetration, high optical power is demanded to penetrate brain tissues to a specific depth. The relationship between the luminance of the Tyndall µLED and tissue penetration depth is shown in Figure 3.9 and Table 3.5. It can be observed that for a basic 100 µm penetration depth, it requires a luminance of 10 µW from the µLED. If the required tissue penetration depth is expanded to 200 µm, the required luminance will increase to 45 µW. And it is sometimes desirable to achieve more than 300 µm penetration in clinical applications [121], in which case a µLED luminance of 105 µW is needed.

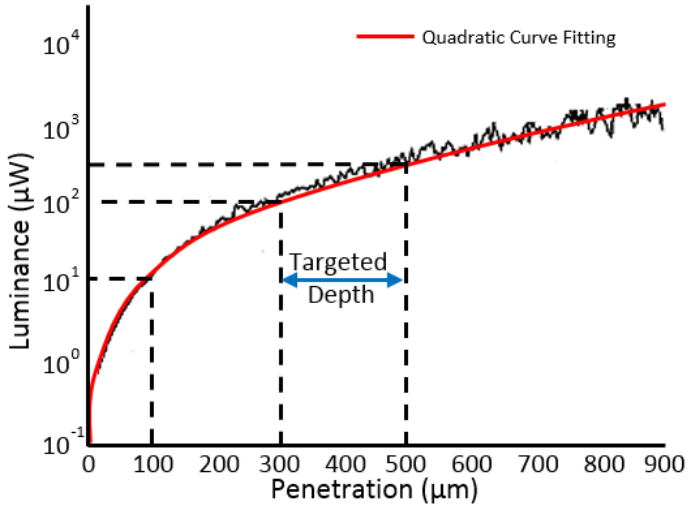


Figure 3.9 Correlation between Tyndall µLED luminance and tissue penetration depth, which corresponds to a quadratic relationship. The expected penetration depth should be ≥ 300 µm. The original data is provided by my collaborator, Mr Na Dong, from Southeast University, China. This figure is modified from [121].

Table 3.5 Targeted tissue penetration depth with required µLED luminance and luminance intensity.

Penetration Depth (µm)	**100**	**200**	**300**	**400**	**500**
Luminance (µW)	10	45	105	240	380
Luminance Intensity (mW/mm^2)	31.85	143.31	334.39	764.33	1210.2

Based on the *I-V*-L relationships depicted in Figure 3.8, the requirements of maximum driving current and voltage for all three types of LEDs are deduced in Table 3.6. This provides a baseline for LED driver design. To achieve 105 µW luminance for 300 µm tissue penetration, the maximum driving current of the Tyndall LED should be 0.97 mA with a 3.58 V voltage across the LED terminals; and the requirements for the Panasonic µLED and the Maplin LED are 1.35 mA, 2.59 V and 1.5 mA, 2.33 V respectively. This requires an appropriate common LED driver which can generate the targeted current/voltage for all three types of LEDs.

Table 3.6 The required maximum LED driving current and voltage for 105 µW luminance.

LED Type	**Max Current (mA)**	**Max Voltage (V)**
Tyndall	0.97	3.58
Panasonic	1.35	2.59
Maplin	1.5	2.33

Luminance Controllability

While achieving the targeted luminous intensity from the proposed implant, it will also be advantageous to develop a new type of µLED driving circuit which holds strong intensity controllability. To date for most existing optogenetic implants, the adjustments of light intensity are attained by externally tuning the stimulation operation cycle and/or manually changing the power supply. However, these methods can only realise a limited modulation of light intensity. Therefore, a programmable intensity modulation scheme is desired for the proposed new optrode design. An accurate intensity modulation scheme could guarantee the precision of light delivery, and would also improve operational efficiency. Besides this, with stronger light intensity controllability, safer and more reliable optical stimulation could be obtained. In order to optimise luminance controllability, the modulation scheme should be able to regulate both the optical stimulation cycle and the µLED driving current/voltage. This would achieve an outstanding overall luminance intensity modulation. Thus, an appropriate pulse width modulator needs to be developed which can define and tune the stimulation cycle with high temporal resolution. In the meantime, intensity magnitude control methods are expected to be achieved by incorporating particular data conversion and/or amplification structures.

3.5.3 Spatiotemporal Resolution

As mentioned above, the proposed optrode aims to be applied in extensive brain circuitry for multi-site/multi-layer stimulation. This needs a reasonable level of spatial resolution for each stimulation site. As demonstrated in Figure 3.5, multiple µLED sites will be constructed and evenly positioned along the optrode shaft, and the targeted spatial resolution should be defined at micrometre scale. This requires µLED bonding pads with small dimensions ($\leq$ 100 × 100 μm^2) and a reasonable spacing between each two µLED points ($\leq$ 50 µm).

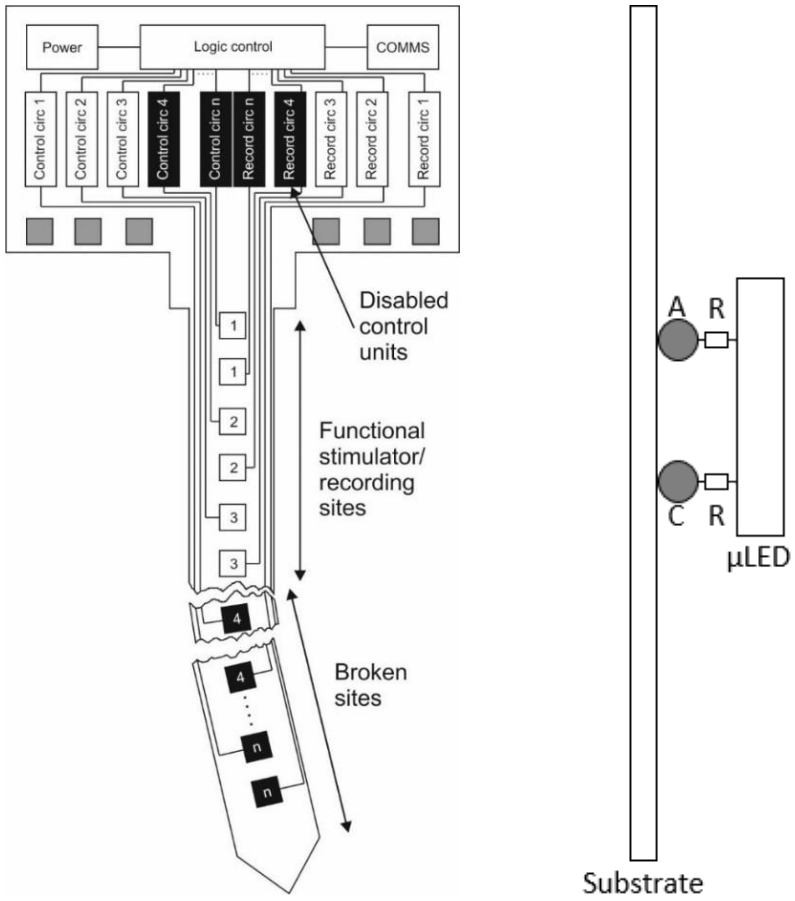
For optogenetic stimulation, the operation frequency is usually in the Hertz scale, typically between 10 - 20 Hz. In this scenario, a high-frequency configuration is not demanded. However, it would be helpful to ensure that the µLED drivers can sustain relatively high frequency signals (KHz or MHz) in order to maintain sufficient margins. Although for CANDO project the typical stimulation cycle will be in the millisecond range, this may be potentially beneficial for high-frequency applications in the future.

3.5.4 Biphasic Stimulation

Biphasic stimulation topologies have been widely used for charge-balanced electrical stimulation [122]. For optical stimulation, the function of biphasic stimulation is different. Although charge balance issues are not taken into account, a biphasic control pattern is still beneficial for optical neural stimulation. Firstly, by incorporating biphasic control pattern, the system will be flexible to switch the µLED working state from forward biased to reverse biased. This could be helpful in the investigation of electrical characteristics of reverse biased µLEDs. In particular, based on the linear relationship between LED reverse current and temperature, it would be useful for a future design of a µLED-based temperature sensor, which can help to investigate the local thermal effect of using the µLED itself. Moreover, this bidirectional configuration can avoid the potential problem of degeneration caused by the electric field between the µLED anode and the common ground. Besides this, the biphasic control topology can be configured for both optical stimulation and diagnostic sensing. Hence, the biphasic control pattern is demanded to be incorporated into optogenetic applications for the first time.

3.6 Self-Diagnostic Function

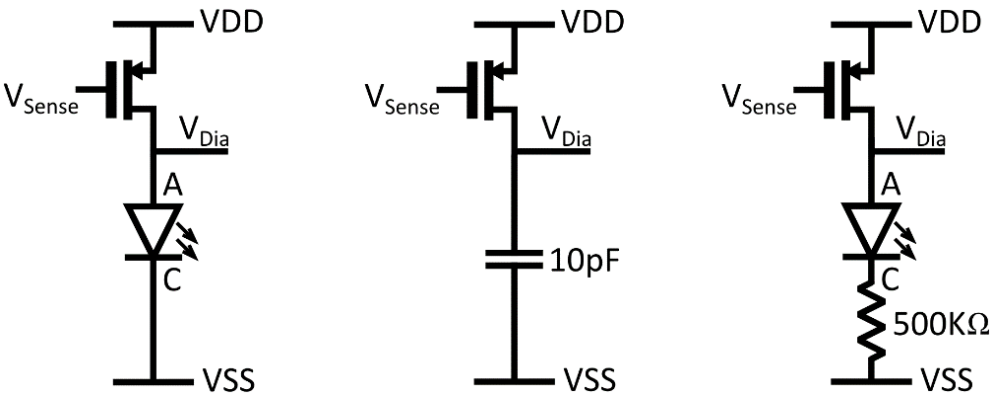
For implantable applications, safety always has the priority. One risk with this implant is shaft breakage occurring during or after implantation, as illustrated in Figure 3.10. An advantage of the proposed active optrode is that, because of the individual controlling scheme, stimulation sites above the area of breakage can still be functional while other stimulation sites are disabled. However, it is important and necessary to construct particular sensing circuitry to assess the integrity of the implant. If any breakage happens, depending on its severity, either the faulty component could be switched off and redundant light emitters could then be switched on, or the optrode could be entirely shut down. This can avoid unnecessary power consumption and, more importantly, can inhibit unexpected current being injected into brain tissue. Another danger which may occur during the implant operation is the long-term operational degradation of the stimulation site. Contact corrosion between the CMOS circuitry and the µLED is a major concern. When severe erosion happens, the behaviour of the light emitters is distorted, which can bias the predefined light delivery. Thus, it is also essential to create a sensing mechanism to evaluate the operational degradation status of the light emitters.



(a) (b)

Figure 3.10 (a) Conceptual diagram showing a breakage in the optrode shaft. As the stimulation sites are individually controlled, stimulation sites below the damaged region are disabled, whereas stimulation sites above the damaged region can operate as normal. (b) A conceptual diagram demonstrates the contact corrosion happens between the CMOS substrate and the µLED. *A* and *C* represent the anode and cathode of the µLED. Under the contact corrosion status, the serial resistances *R* of the bonding site are increased.

In order to investigate these abnormal operation conditions, equivalent circuit models have been generated as displayed in Figure 3.11. A PMOS transistor is selected to perform as a control switch of the µLED. When the µLED is under normal operation, it performs with diode-like behaviour. If, however, there is a rupture occurring at the optrode shaft, an open circuit is then formed in the vicinity of the stimulation site. This open state can then be mimicked by a capacitor, as shown in Figure 3.11 (b). When contact erosion occurs at the stimulation site, a significant resistance is then generated, which makes the diode performance more resistive. This resistive state can be modelled by a serial resistor, as displayed in Figure 3.11 (c). All these three different operational states can be expressed via the voltage across the µLED anode terminal.



(a) (b) (c)

Figure 3.11 Equivalent circuit models of three µLED operation states. A PMOS transistor (10 µm/1 µm) is acting as a control/sensing switch of the LED. (a) Normal condition. (b) Optrode breakage, where a 10 pF capacitor is connected to replace the µLED to mimic the broken optrode. (c) Contact corrosion between the CMOS circuitry and the µLED bonding pad, and a 500 KΩ resistor is used to mimic the increased sheet resistance caused by contact erosion.

By tuning the gate voltage V_{Sense}, the PMOS transistor can generate specific sensing current to the µLED. This sensing current will vary quadratically to provide a wide dynamic range. Consequently, a diagnostic voltage V_{Dia} will then be generated across the µLED. The comparison analysis in Figure 3.12 demonstrates how V_{Dia} is expressed when $|V_{gs}|$ (e.g. V_{DD} - V_{Sense}) is gradually increased from 0 V to V_{DD}. In the normal condition, the µLED behaviour is illustrated by the green curve. It can be seen that the µLED is firstly under a transistor-dominated sub-threshold state; after that, it reaches a µLED sub-operation area, and there is no light emitted; and it finally arrives at the saturation region of the sensing transistor. In contrast, when an optrode breakage happens, an open circuit is then created, and V_{DD} directly falls down to the breakage point. In the scenario of contact erosion, massive resistance is generated between the CMOS circuitry and the µLED, which will exhibit a more resistive behaviour; the µLED mainly behaves like a diode at the start; then it becomes significantly resistive, and V_{Dia} is dramatically increased until saturated with V_{DD}.

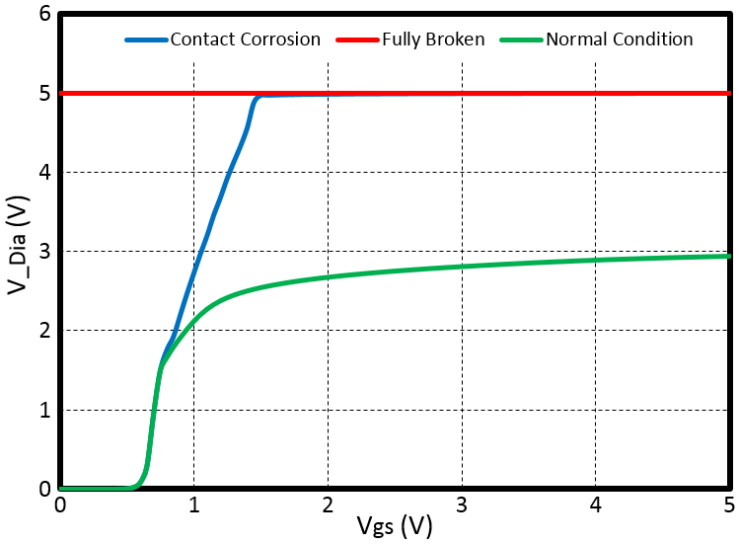


Figure 3.12 Comparison analysis of three LED operational conditions. $|V_{gs}|$ is equal to V_{DD} - V_{Sense}. The green curve represents the normal condition which performs typical diode-like behaviour. The red line indicates that, when shaft breakage exists, an open circuit will then be formed at that point. The blue curve demonstrates a more resistive status when contact erosion occurs between the CMOS circuits and the light emitter.

This comparison modelling analysis indicates that, by extracting the voltage profile of the µLED, the optrode operational status can be tracked in real-time. This provides the basic design principle for the diagnostic sensing circuitry. Therefore, in order to realise the self-diagnostic function, particular sampling points of V_{Sense} needs to be predefined to achieve the voltage sweeping of the sensing transistor. Then a corresponding diagnostic voltage V_{Dia} will be generated across the µLED, expressing the real-time status of the stimulation site. If any abnormality exists, it could be automatically observed by recording the voltage at that point. To accomplish this sensing scheme, data conversion structures and amplification stages are required for voltage/current scanning and data recording. The diagnostic function can only operate in 'dark' mode, i.e. µLEDs are not turned on and no light is emitted. This requires a 'weak' diagnostic current to sense the stimulation site, and based on the suggestion from clinical staff, this current should be limited at the µA scale (i.e. 50 µA or lower), in order to ensure the patient safety.

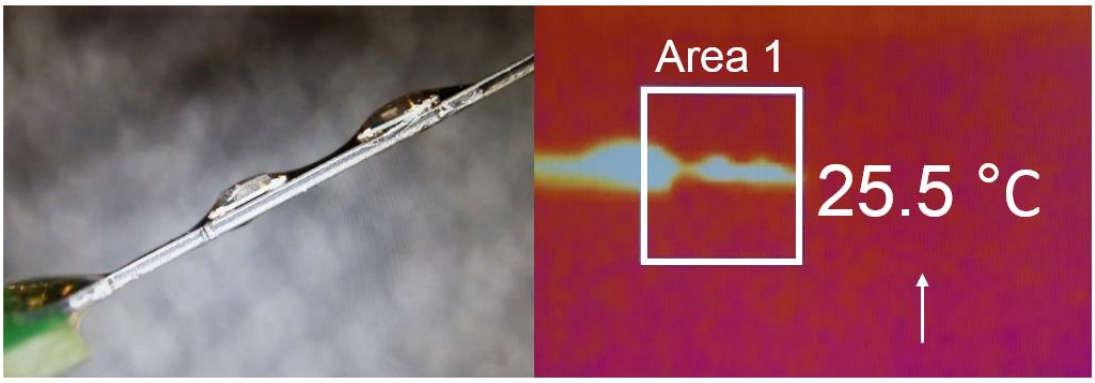
This diagnostic mode will be firstly operated after insertion. It can then be run periodically to check the optrode condition. Alternatively, it may be run on demand; for instance, during a patient consultation with a clinical physician or technician. This self-diagnostic sensing strategy can significantly enhance the system safety and long-term durability.

3.7 Thermal Analysis and Sensing

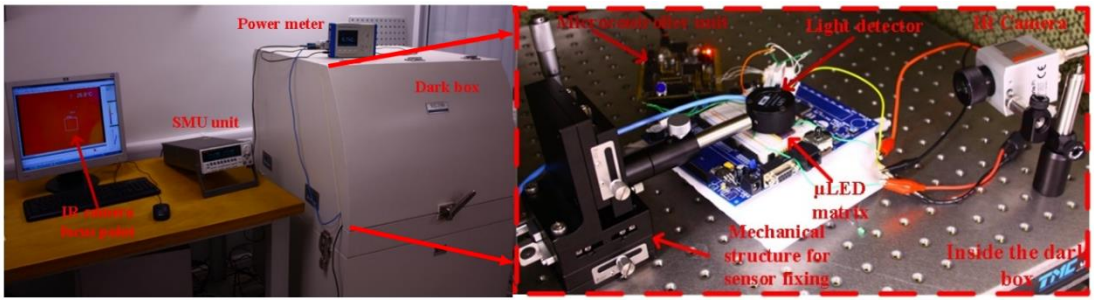
Thermal dissipation from the device to the surrounding tissue is crucial for implantable optical stimulation. In particular, for the µLED-on-optrode structure, the light source is directly inserted into brain tissue, generating local heating. Based on the regulations concerning heating dissipation of implants [112-114] formulated by the US FDA and UK Medicines and Healthcare Products Regulatory Agency (MHRA), the temperature of the implant surface cannot be increased by more than 2 ℃ beyond the default body temperature. Thus, it is essential to investigate the thermal effects of light emitters both before and after optrode fabrication.

Thermal Analysis

Therefore, in parallel with optrode development, a physical thermal measurement of a purely silicon-based optrode prototype has been conducted (by my colleague Dr Ahmed Soltan at Newcastle University), as illustrated in Figure 3.13. In this silicon probe, there is no functional circuitry, and only two Panasonic µLEDs are bonded to it. The geometry of this testing probe is defined and constructed as per the pattern provided in Figure 3.5, ensuring the accuracy of measurement results. In this thermal experiment, different amounts of electrical power are given to continuously drive the µLEDs, and a detailed series of transient thermal tests have been performed. The measurement results are displayed in Figure 3.14.



(a) (b)



(c) (d)

Figure 3.13 Thermal measurement set-up. (a) A silicon-based testing optrode with no functional circuits included, and only two µLEDs are bonded to it for thermal analysis. (b) This testing probe is driven by predefined electrical power levels, and the local temperature is captured by an infrared camera. (c) The thermal test platform, where a dark chamber is utilised for thermal/optical isolation. (d) Inside the dark chamber. This figure is modified from [121].

It can be seen that the temperature increment is around 4 °C (from the base temperature of 23 °C to ~27 °C) within two minutes measurement under 41 mW electrical power, and this indicates an increasing trend in the temperature profile. If, however, the power is reduced down to 13 mW, the temperature rise can be saturated within 1.6 °C, and this meets the regulation stated in [112-114]. When the total input power is further reduced to 6.0 mW, the thermal increment of the light emitters is limited to 0.8 °C. And with 3.0 mW power, the temperature rise can be cut down to 0.4 °C.

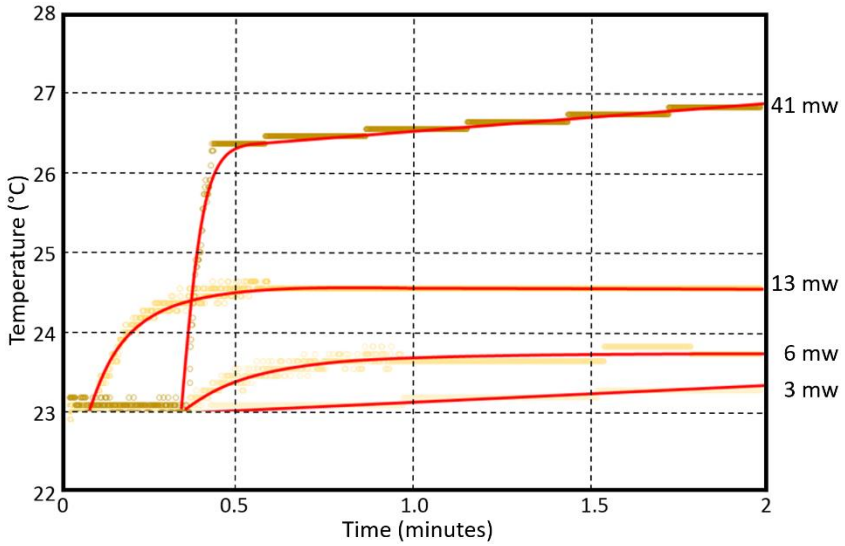


Figure 3.14 Transient thermal measurements of the silicon-based testing probe. The ambient temperature is 23 °C. The test period is 2 minutes. During each measurement, LEDs are continuously driven by predefined electrical power from 3 mW to 41 mW. From 0 minute to 0.5 minute, there are some response delays caused by the measurement equipment. This figure is modified from [121].

From the thermal analysis described above, it is clear that the μLED power needs to be appropriately modulated, to constrain the thermal effect within a reasonable range. If aiming to limit the temperature rise to within 2 °C, it is useful to set the continuous μLED power to no more than 13 mW. Moreover, in order to ensure safer operation, it is desirable to restrict the thermal increment to within 1 °C, in which case the light emitters should not be continuously driven with more than 6.0 mW power. This thermal analysis provides a clear criterion for light power controlling. It further highlights the importance of the light power/luminance controllability of the proposed implant, as stated in Section 3.5.2. Hence, as mentioned above, an advanced programmable light power/luminance modulation mechanism is a strong requirement. This can not only improve stimulation efficiency and achieve finer overall intensity modulation, but would also regulate the thermal effect of the light emitters within a safe and healthy range.

Thermal Sensing

Apart from the control method proposed above, it is worth incorporating specific sensing structures into the optrode further investigate and monitor the temperature of each stimulation site. Suitable temperature sensors should be built into the implant so as to observe the in-situ temperature of the light emitter. Therefore, a miniature thermal sensing structure needs to be developed, which can be fitted at/close to each stimulation site. Once the risk of overheating is detected, either the light power should be correspondingly adjusted, or that specific light emitter can be cooled off. By incorporating both thermal controlling and sensing methods, the heating dissipation in this optogenetic implant could be effectively managed.

3.8 Electrical Neural Recording

As explained in Chapter 2, the closed-loop neuromodulation system is a new trend in neuroprosthesis applications. Recently, electrical neural recording circuitries have been increasingly developed and integrated into neural stimulators to accomplish closed-loop neural interfaces. In particular, for implantable optogenetic stimulation, it is very useful to observe local neural activities using neural recording components. Real-time feedback signals can be provided to the optical stimulator, and these observed neural signals could provide accurate operation criteria for the optogenetic

stimulator. These would determine whether to trigger a specific light emitter for local light delivery, and could be helpful for setting and adjustment of the appropriate stimulation cycle and intensity. From a circuit design perspective, although neural recording is presently a hot research topic, it is not a focus of this thesis. However, from a system implementation perspective, it is sensible to integrate existing electrical neural recording circuitry [123, 124] into this new type of optogenetic implant, constructing a novel closed-loop optical-electro neural interface.

3.9 Power Budget

The proposed optrode would be powered by a rechargeable battery in the first instance. The capacity of the battery is 600 mAh [121], and the 80% recharge period is set to be no less than 36 hours. It turns out that the total power consumption of the implant and the chest unit cannot be greater than 44 mW. In particular, 30 mW power budget is reserved for the chest biomedical processor, and then the maximum total power consumption of the optrode is 14 mW. Moreover, the continuous light power must be limited to 13 mW.

3.10 Conclusion

This chapter has proposed a new type of optogenetic implant using direct µLED-on-CMOS technology. Diverse functioning circuitries will be developed and incorporated into the implant to accomplish a multi-functional closed-loop optical-electro neural interface. A conceptual design and system floorplan have both been illustrated, and general design specifications have been defined and elaborated. A specifications summary of the proposed optogenetic implant is displayed in Table 3.7.

Most of existing optogenetic implants, have been custom-fabricated, which results in relatively high costs and extensive working loads, as well as limiting their wider adoption and application. In this new proposed optrode design, 0.35 µm commercial CMOS technology is chosen for optrode fabrication. As a widely-used semiconductor fabrication process, the CMOS process will be more cost-efficient labour-less than custom fabrication/post-processing. Moreover, it will be highly flexible for other researchers to adapt for a range of broader applications.

For the optical implant, the main function is to accurately and reliably deliver specific light into tissue areas of interest. This requires finer light drive capability and controllability. The targeted luminance has been defined as 105 μW to realise the expected penetration depth. Programmable light intensity modulation schemes are demanded to offer more precise and efficient light emission. This will also be helpful for thermal management. In particular, a suitable pulse width modulator is needed to regulate the stimulation operation cycle at high resolution, while specific data conversion and amplification modules are required to achieve intensity magnitude controlling. Besides this, for recent optogenetic applications, multi-site/multi-layer stimulation is increasingly required for applying into large brain networks. Therefore, the appropriate spatial resolution of multiple stimulation sites needs to be defined. In addition, the biphasic stimulation control pattern would be explored and employed into this optogenetic implant, in order to configure both optical stimulation function and diagnostic sensing operations. This could also be beneficial for future research.

A vital risk with implantable applications is the integrity and long-term durability of the implant. It is important to incorporate specific sensing circuitry to monitor its operational status in real-time. Both implant rupture and contact degradation should be observed by extracting the voltage profiles of the light emitters. This requires a voltage/current scanning scheme to define specific sensing sampling points, and a corresponding readout module is also needed to decode and fetch the diagnostic output. In particular, this self-diagnostic operation should be performed in ‘dark’ mode, after implantation and between stimulation operations.

Thermal effect is another concern with implantable applications. Based on the present regulations [112-114], the implant temperature rise cannot exceed 2 ℃. This needs suitable light power regulations. In order to control the thermal increment to within 2 ℃ (1.6 ℃), light emitters cannot be continuously powered with more than 13 mW. If it is intended to further constrain the maximum temperature increase to below 1 ℃, the continuous light power cannot be above 6 mW. This requires that each stimulation site should be suitably duty-cycled, and the light intensity could be dynamically adjusted. Meanwhile, thermal sensing components are demanded to be placed close to each stimulation site, to further prevent the overheating hazard.

In addition, the proposed optrode design should be compatible with electrical neural recording circuitry. Existing recording system [123, 124] should be able to be fitted into the optogenetic implant to complete the multi-functional closed-loop neuroprosthesis system.

All of these requirements need to be fulfilled using specific CMOS circuits. Chapter 4 details diverse circuit designs and demonstrates how these circuits meet the requirements proposed above.

Table 3.7 Specifications summary of proposed optogenetic implant.

System Parameters	
Fabrication technology	AMS (X-Fab) 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V, 5.0 V
Power budget	14 mW (system)/13 mW (continuous light)
Optrode head dimensions	1000 µm × 2000 µm
Optrode shaft dimensions	4000 µm × 300 µm
Subsystems	stimulation, diagnostic, thermal, recording
Optical Stimulation	
µLED current range	0 - 1.5 mA
µLED voltage range	0 - 3.6 V
Targeted light luminance	≥ 105 µW
Targeted light intensity	≥ 334.4 mW/mm^2
LED driving mode	Mono-direction/Bi-direction
Intensity modulation methods	PWM, intensity magnitude control
No. of stimulation sites	6
Diagnostic Sensing	
Input sensing current	0 - 50 µA
Output diagnostic voltage	0 - 3.3 V/0 - 5 V
No. of sensing sites	6
Thermal Sensing	
No. of sensing sites	6
Neural Recording	
No. of recording sites	4

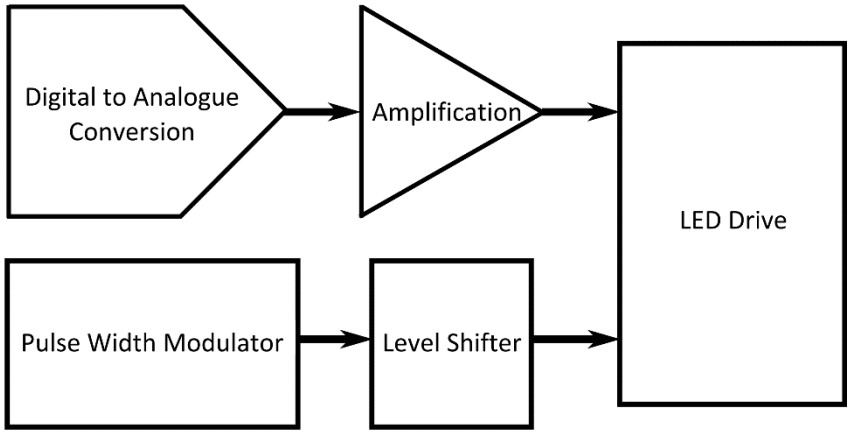
Chapter-3 Contributions

Contributor	Contributions
Mr Hubin Zhao	1) Defined the system architecture of the optrode 2) Investigated the appropriate fabrication process 3) Investigated the physical characteristics of μLEDs and analysed &characterised the *I-V-L* features of different types of LEDs 4) Deduced and defined the targeted luminance driving ability and controllability 5) Investigated the biphasic optical stimulation control pattern 6) Investigated the self-diagnostic strategy 7) Investigated and analysed the thermal effect light emitters 8) Defined the optrode power budget
Dr Patrick Degenaar	1) Suggested the general concept of the optrode in Figure 3.1 2) Provided related research resources from the OptoNeuro project and the CANDO project
Dr Ahmed Soltan	Conducted the thermal measurement the silicon-based testing probe, in Figure 3.13
Mr Na Dong	Provided the original data of the Tyndall μLED tissue penetration depth, in Figure 3.9

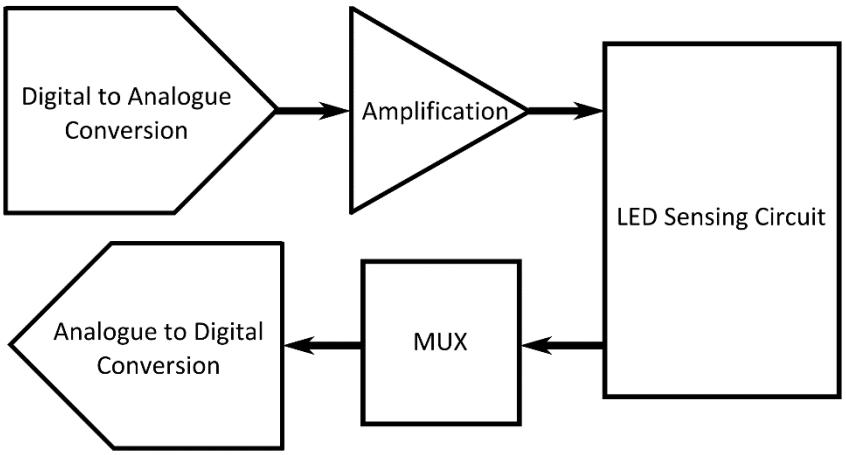
4 Circuit Design

4.1 Introduction

As mentioned in the previous chapter, the proposed optrode requires high current to drive the µLEDs so as to obtain the targeted light intensity for local light delivery. The µLED light intensity should be adjustable, and it should have a wide dynamic range that typically varies from zero to 300 mW/mm^2 or more. Furthermore, it is important to include in-built sensing circuitry to detect operational abnormalities such as contact corrosion between the µLED and CMOS circuit and/or substrate breakage, post implantation or during optrode operation. Therefore, this chapter presents two key circuitry designs for the proposed optrode: the optical stimulation circuitry and self-diagnostic sensing circuitry. In the optical stimulation circuitry, monophasic and biphasic stimulation control approaches are analysed, compared and developed simultaneously. PWM control and intensity magnitude control schemes are employed to get finer overall intensity modulation. In the diagnostic sensing circuitry, a voltage-current scanning approach is investigated to formulate the voltage profile of the µLED in the standby state, when the µLED is driven by a weak current in different scenarios. This strategy makes real-time abnormality identification possible, which will significantly enhance operational safety and reliability.



(a)



(b)

Figure 4.1 Simplified development flow charts of optical stimulation circuitry and diagnostic sensing circuitry. (a) The optical stimulation circuitry primarily includes digital to analogue conversion stage, amplification & inversion stage, PWM module, and related peripheral components (b) The diagnostic sensing circuitry mainly consists of digital to analogue conversion stage, amplification & step-up module, analogue to digital conversion block, and supplementary elements.

The basic flow charts for the development of the optical stimulation circuitry and diagnostic sensing circuitry are demonstrated in Figure 4.1. In the former, digital to analogue converter (DAC) and amplification stages are required for light intensity control. In the meantime, a pulse width modulator is needed to realise the pulse width modulation (PWM) control of light emission. Accessory elements are incorporated, such as a level shifter and serial to parallel (S-to-P) interface, to complete the system. In the diagnostic sensing circuitry, another separate DAC is included to generate the weak diagnostic sensing current and to provide the voltage-current scanning mechanism. A dedicated amplifier is designed to convert 0 - 3.3 V DAC output into a µA-level current. An analogue to digital converter (ADC) is employed to record the sensed diagnostic results. Supplementary elements are utilised to complete the diagnostic circuitry, including a S-to-P interface, a parallel to serial (P-to-S) interface, a multiplexer (MUX), and a demultiplexer (DEMUX).

This chapter includes two main sections followed by a conclusion section. Section 4.2 details the circuitry designs needed for both the stimulation function and diagnostic operation. Section 4.3 elaborates on all of the dedicated components used for the diagnostic sensing circuitry. Section 4.4 concludes this chapter.

4.2 Optical Stimulation Circuitry

4.2.1 Introduction

The general system architecture of the stimulation circuitry is illustrated in Figure 4.2. It primarily consists of four parts: µLED drive circuitry, pulse width modulator, intensity modulation circuitry and accessory analogue/digital cells. All of the required modules are listed below, and they are utilised to construct the optical stimulation circuitry while some of them are applied in the diagnostic sensing circuitry (such as DAC and S-to-P Interface).

- µLED Driver
- Pulse Width Modulator
- Inverting Voltage Amplifier
- Digital to Analogue Converter
- Serial to Parallel Interface
- Level Shifter

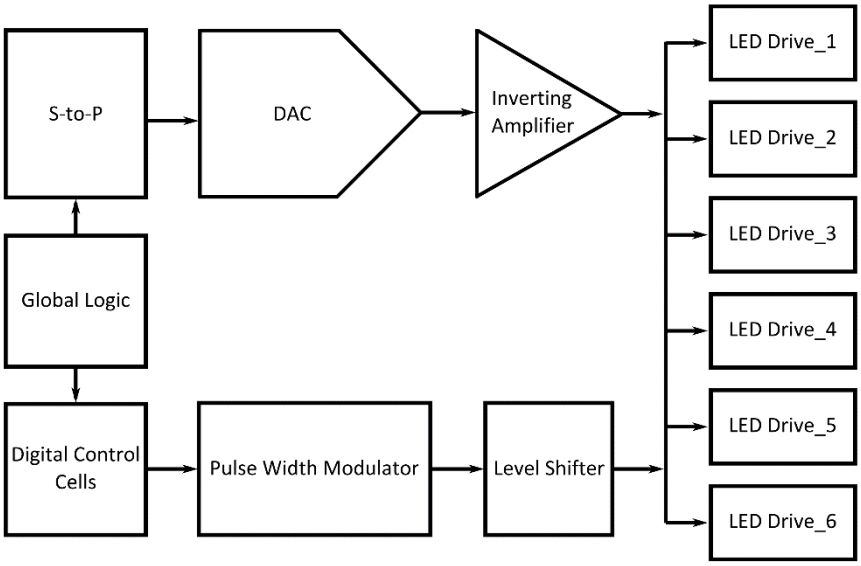


Figure 4.2 General architecture of the optical stimulation circuitry. It mainly consists of µLED drive, pulse width modulator, inverting voltage amplifier, DAC, S-to-P interface, and level shifter. Global control logic and accessory digital cells are utilised for logic control and data communication.

This section is organised as follows. Detailed design and analysis of the µLED drive circuitry are presented in Subsection 4.2.2. Subsection 4.2.3 investigates the controlling and modulation mechanism of light intensity, and two feasible methods

(PWM and intensity magnitude control) are utilised to attain programmable intensity adjustment. Subsection 4.2.4 details the development of the pulse width modulator. And the following subsection describes the implementation of a particular inverting voltage amplifier. Then, different design strategies for DAC modules are explored in Subsection 4.2.6. Designs of the S-to-P interface and level shifter are illustrated in Subsection 4.2.7 and 4.2.8 respectively. Subsection 4.2.9 provides a summary of the optical stimulation circuitry development.

4.2.2 µLED Drive Circuit

In this subsection, both monophasic and biphasic µLED drive circuits are investigated and developed. In the first part, basic CMOS transistor characteristics are inspected to define the µLED drive transistor. Next, the monophasic drive circuit is constructed as the first version of the µLED drive circuit. In the third part, two versions of biphasic drive circuits are proposed and implemented for optical stimulation.

4.2.2.1 PMOS and NMOS

In the µLED drive circuit, a wide metal-oxide-semiconductor field-effect transistor (MOSFET) is used as the drive transistor to generate high current flow. The drive transistor can be either an n-type MOSFET (NMOS) or a p-type MOSFET (PMOS), as shown in Figure 4.3.

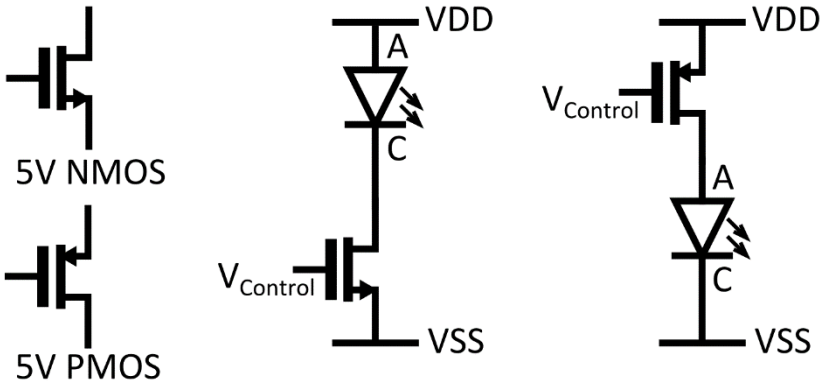


Figure 4.3 µLED Drive Transistors. (a) 5 V NMOS and PMOS symbols. (b) n-type µLED drive transistor. (c) p-type µLED drive transistor.

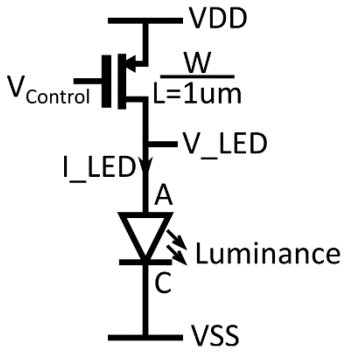
Assuming that the NMOS is selected as a µLED drive transistor, when the control voltage $V_{control}$ is 0.0 V then the NMOS maintains off, and no current passes through

the drive transistor to the µLED. When the control voltage reaches the maximum supplied voltage (usually V_{DD}), the NMOS is fully open, and the expected utmost current will then be generated. The operation of the PMOS is inverse to that of the NMOS, i.e. when $V_{Control} = V_{DD}$ there is no current passing through the µLED, and when $V_{Control}$ = 0 V the current through the µLED reaches its upper limit. Thus, theoretically, both the NMOS and PMOS can be utilised as a drive transistor. However, considering future applications such as a high-density µLED array for visual cortex prostheses, common n-terminals need to be configured in the µLED array. To retain this possibility, the P-type transistor is chosen here as the µLED drive transistor.

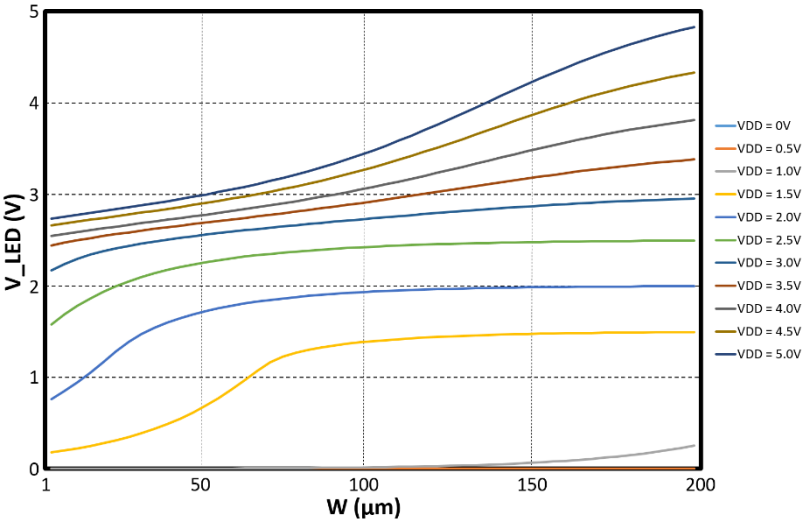
Since the targeted range of µLED operating voltage (the voltage drop between the µLED anode and cathode) is from 0 V up to 3.6 V, as mentioned in Chapter 3, Section 3.5, a standard 3.3 V transistor is not suitable. In order to fulfil the requirements described above, a 5 V transistor is then selected as the µLED drive transistor. The 5 V drive transistor can potentially provide a voltage drop of 4 V (or more) across µLED, matching the targeted working voltage range (0 - 3.6 V) and making the µLED driving ability more scalable.

4.2.2.2 Monophasic Drive Circuit

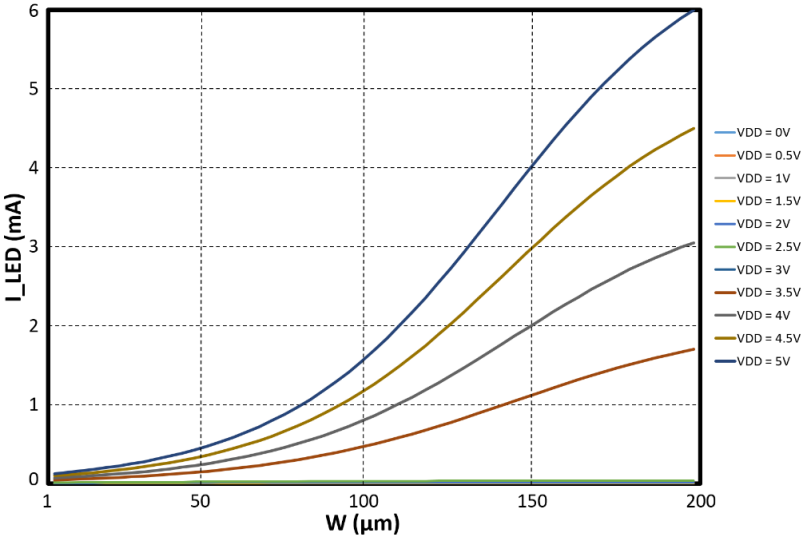
Therefore, a 5 V PMOS transistor is utilised in the monophasic drive circuit, as illustrated in Figure 4.3 (c). The width/length ratio of the drive transistor determines the maximum current through the µLED drive circuitry, when the power supply is constant. In order to generate the desired high µLED current, the default length of the drive transistor is defined as 1 µm, and the width needs to be set. Figure 4.4 shows the parametric analysis result for the drive transistor, obtaining the channel width (W) - voltage across the µLED (V_{LED}) and the channel width (W) - channel current I_{DS} (I_{LED}) relationships respectively. The power supply varies from 0.0 V to 5.0 V with 0.5 V steps. To note, all of the simulations conducted in this chapter are based on Panasonic µLED unless otherwise specified.


VDD
W
V_Control
L=1um
V_LED
I_LED
A
Luminance
C
VSS

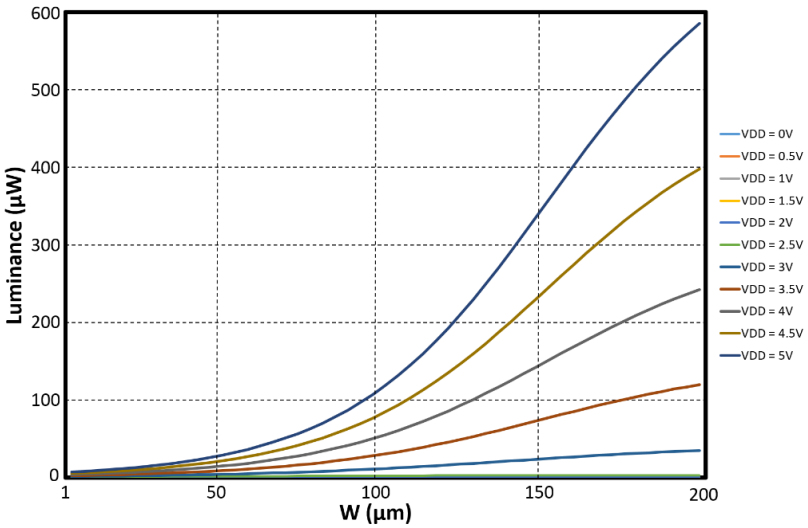
(a)


V_LED (V)
W (µm)
VDD = 0V
VDD = 0.5V
VDD = 1.0V
VDD = 1.5V
VDD = 2.0V
VDD = 2.5V
VDD = 3.0V
VDD = 3.5V
VDD = 4.0V
VDD = 4.5V
VDD = 5.0V

(b)


I_LED (mA)
W (µm)
VDD = 0V
VDD = 0.5V
VDD = 1V
VDD = 1.5V
VDD = 2V
VDD = 2.5V
VDD = 3V
VDD = 3.5V
VDD = 4V
VDD = 4.5V
VDD = 5V

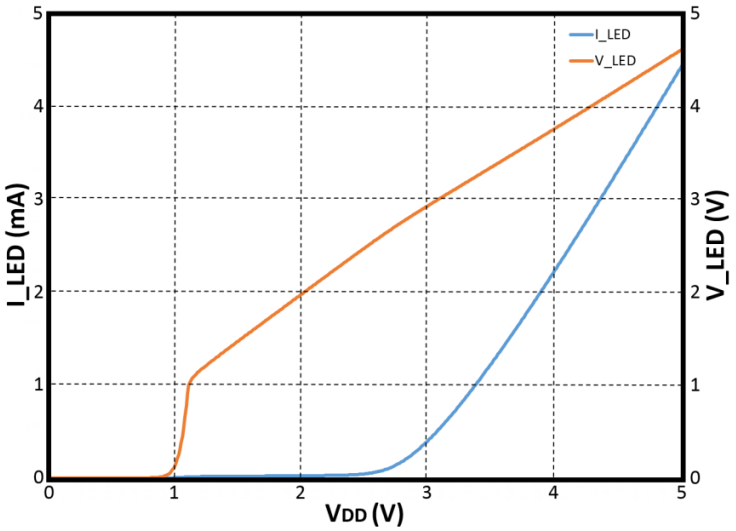
(c)



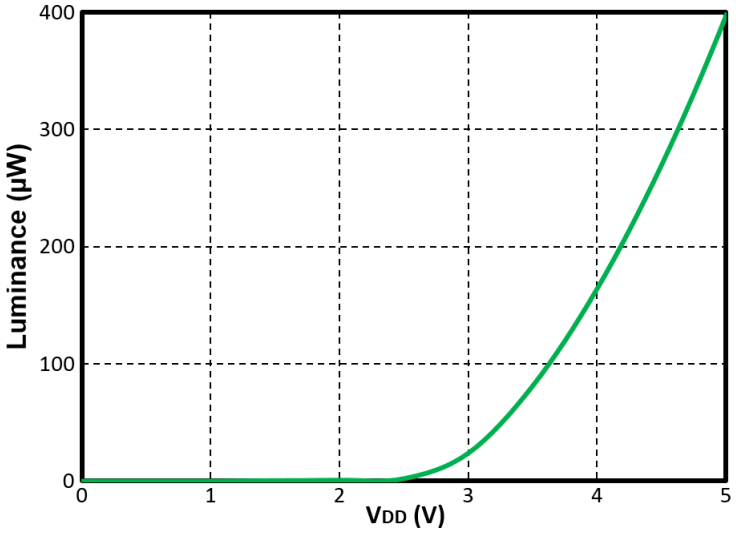
(d)

Figure 4.4 (a) Equivalent circuit of the monophasic drive circuit. (b-d) Parametric analysis results of *W* - V_{LED} (b), *W* - I_{LED} (c) and *W* - *Luminance* (d) relationships. *W* is swept from 1 µm to 200 µm, and V_{DD} is changed from 0 V to 5 V. It can be seen when V_{DD} is 5.0 V and *W* is greater than 100 µm, the *Luminance* meets the design requirement (≥ 105 µW).

It can be seen that a wider transistor could supply a higher voltage drop across the µLED and a stronger current through the µLED. But this would also increase the circuit area, and the current may potentially be influenced by the process variation of transistor fabrication. Given the trade-off between driving ability and dimensions, the *W/L* ratio of the monophasic drive transistor is set as 160 µm/1 µm, and this drive transistor has been implemented in Chapter 5, Subsection 5.2.3. As depicted in Figure 4.5 below, with 5.0 V V_{DD}, the maximum µLED driving current is 4.4 mA, and the maximum illuminance is 400 µW, which is sufficient for targeted local light delivery.



(a)



(b)

Figure 4.5 (a) µLED *I-V* relationship. When the drive transistor *W/L* is 160 µm/1 µm, with sweeping of V_{DD} from 0 V to 5.0 V. (b) The corresponding luminance curve based on the µLED *I-V* relationship. Circuit schematic is referred to Figure 4.4 (a).

Figure 4.5 also demonstrates that this monophasic drive circuit is capable of operating in the lower V_{DD} region, such as at 4.5 V, 4.0 V, and 3.5 V, which makes the driving ability more tuneable. Monte-Carlo analysis is then conducted to obtain a statistical analysis of I_{LED} current variations when V_{DD} is set to 5.0 V, 4.5 V, 4.0 V, and 3.5 V, and the results are illustrated in Figure 4.6. It can be observed that although the Monte-Carlo analysis demonstrates an appropriate variation range, the influence is not negligible. Since it is hard to avoid process variation due to the nature of the fabrication technology, it is important to make the stimulation circuitry more programmable, so that the effect of variation could be adjusted and minimised.

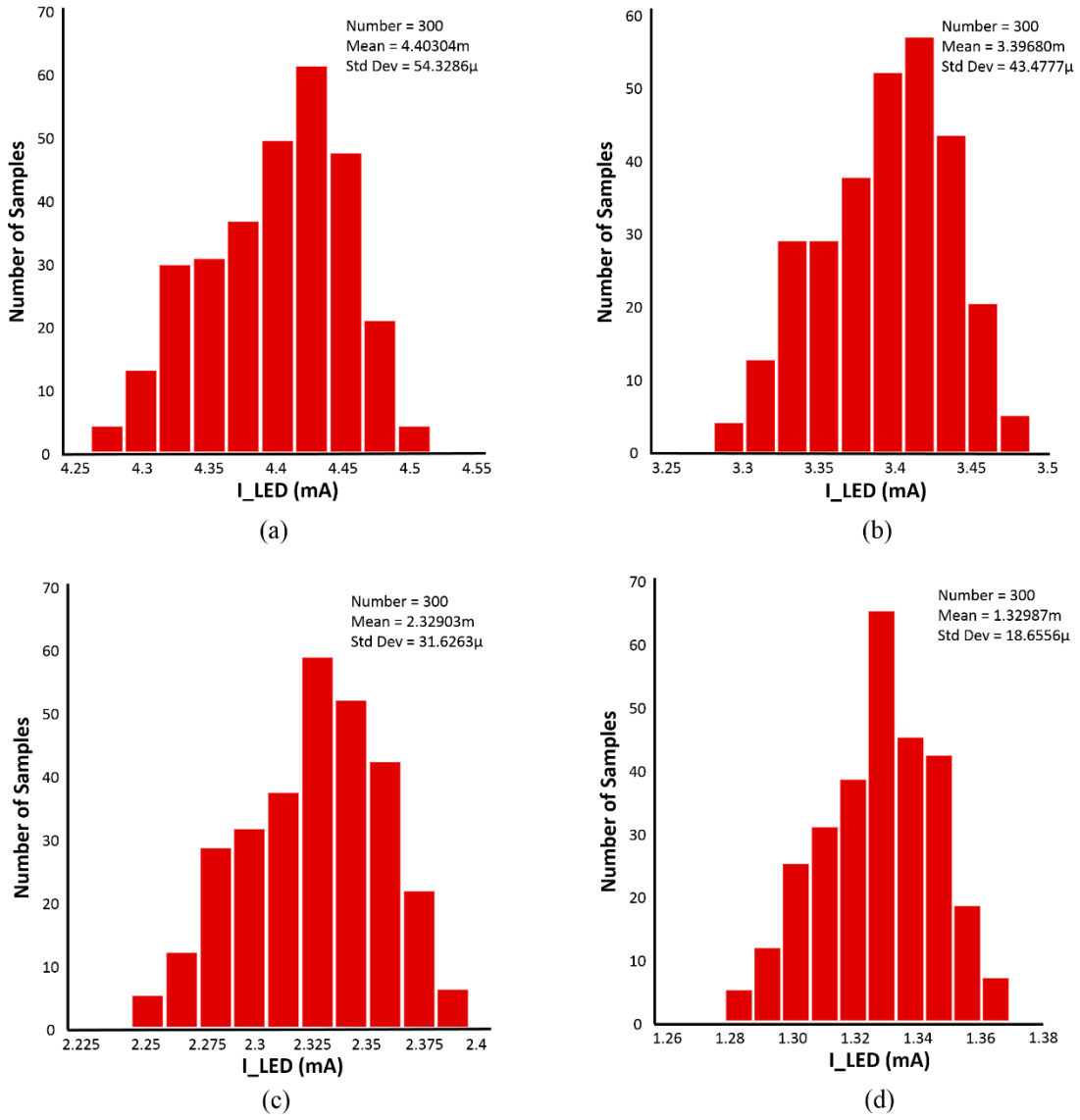


Figure 4.6 Monte-Carlo analysis for I_{LED}. (a) V_{DD} = 5.0 V, I_{LED} varies from 4.27 mA to 4.5 mA, and the mean value of I_{LED} is 4.4 mA. (b) V_{DD} = 4.5 V, I_{LED} is in 3.29 - 3.48 mA range, with a mean value of 3.40 mA. (c) V_{DD} = 4.0 V, I_{LED} fluctuates from 2.25 mA to 2.38 mA, and the average value is 2.33 mA. (d) V_{DD} = 3.5 V, I_{LED} is between 1.28 mA and 1.365 mA, with a mean value of 1.33 mA. Circuit schematic is referred to Figure 4.4 (a).

4.2.2.3 Biphasic Drive Circuit

As depicted in Chapter 3, Subsection 3.5.4, a bidirectional stimulation pattern is needed. The biphasic circuit could allow both light emission and diagnostic settings (as shown in Chapter 5, Section 5.3). A further advantage of the bidirectional stimulation scheme is this configuration can be additionally used to characterise the electrical characteristics of the reverse biased µLED. Moreover, this structure could eliminate potential degeneration caused by the electric field between the µLED anode and common ground.

Therefore, an H-Bridge structure for biphasic optical stimulation is proposed, as displayed in Figure 4.7. Figure 4.7 (a) shows a typical H-Bridge topology which is widely used for charge balancing of electrical stimulation. Here, it has been adapted into Figure 4.7 (b) to drive the µLED bilaterally. It mainly consists of three p-type transistors (P_1, P_2, and P_{Drive}) and two n-type transistors (N_1 and N_2). P_1 and N_1 are connected to the anode of the µLED (point *A*), and P_2 and N_2 are connected to the µLED cathode (point *C*). The main drive transistor is placed at the top of the H-Bridge.

When P_1 & N_2 are turned on, and P_2 & N_1 are switched off, the µLED is set to be forward biased. When P_1 & N_2 are off, and P_2 & N_1 are on, the µLED is in reverse biased mode. P_1 and P_2 are using a 5 V MOSFET so as to have better voltage range, and N_1 and N_2 are with standard 3.3 V transistors (rather than 5 V transistors) in order to reduce the circuit area (N_1 and N_2 are connected to µLED cathodes, and therefore the voltage across the µLED cathodes will never be greater than 3.3 V). Through this configuration, both forward stimulation and reverse stimulation can be accomplished using a single drive source and power supply.

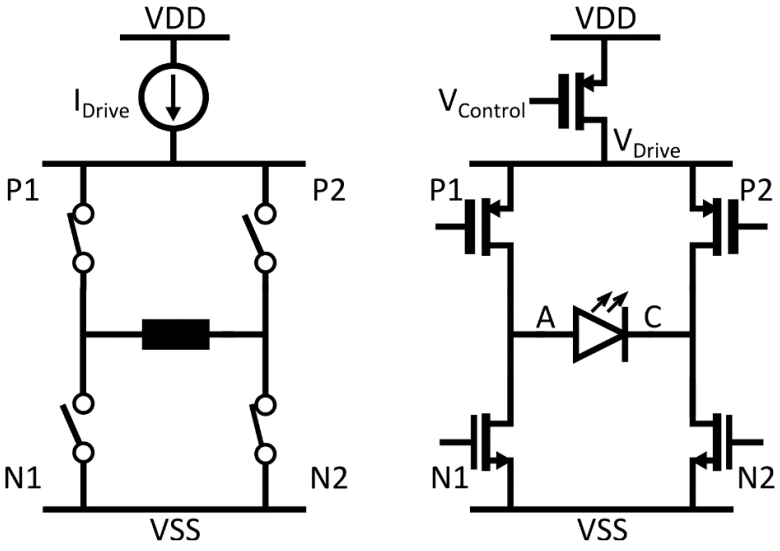


Figure 4.7 H-Bridge. (a) General diagram of H-Bridge topology. (b) An adapted H-Bridge for bidirectional optical stimulation. The top 5 V PMOS transistor is the drive transistor. P_1 and P_2 are two 5 V PMOS transistors, N_1 and N_2 are two 3.3 V NMOS transistors, and these four transistors are acting as switches.

Similar to the monophasic drive circuit, the width/length ratio of the drive transistors determines the light driving ability. The difference is that the monophasic drive circuit is only dominated by a single PMOS, but in biphasic drive circuit the driving ability is constrained by both a PMOS and a NMOS (either P_1 & N_2 or P_2 & N_1). In order to minimise the variations of drive transistors, the lengths of all transistors in this biphasic drive circuit are increased to 2 µm. Based on the targeted luminance driving abilities deduced in Chapter 3, Subsection 3.5.2, the maximum current range is adjusted within the 1.0 - 1.5 mA range (depending on the different LEDs, see Chapter 3, Subsection 3.5.1). After multiple parametric analyses, the sizes of the transistors used in the H-Bridge are specified in Table 4.1, and this H-Bridge has been implemented in Chapter 5, Subsection 5.3.3.

Table 4.1 Transistor dimensions of the H-Bridge in Figure 4.7.

Transistor	P_{DRIVE}	P_1	P_2	N_1	N_2
Dimension	50 µ/2 µ	60 µ/2 µ	60 µ/2 µ	30 µ/2 µ	30 µ/2 µ

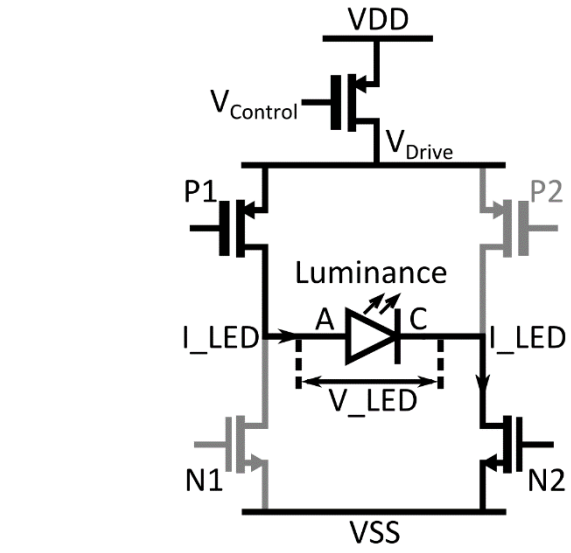
Triode Region Operation vs Saturation Region Operation

Based on the PMOS operation equations displayed below, the operation of the µLED drive transistor can be divided into three different modes: weak inversion mode, triode mode and saturation mode. Based on these three equations, the corresponding relationship between V_{Drive} and $|V_{gs}|$ are depicted, as illustrated in Figure 4.8.

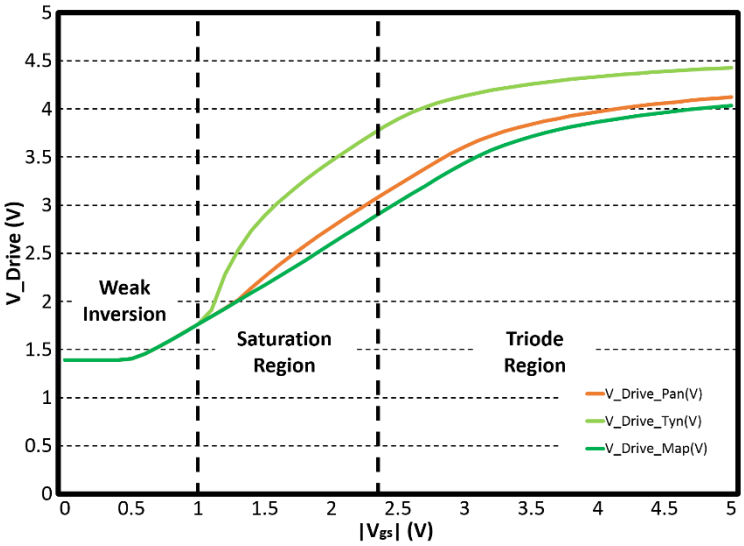
$V_{SG} < V_{THP}$ $$I_D = \frac{W}{L} I_{D0} exp(\frac{qV_{SG}}{nKT}) \quad (4.1)$$

$V_{SG} \geq V_{THP}$ & $V_{SD} \leq V_{SG} - V_{THP}$ $$I_D = K_P \frac{W}{L}[(V_{SG} - V_{THP})V_{SD} - \frac{1}{2}{V_{SD}}^2] \quad (4.2)$$

$V_{SG} \geq V_{THP}$ & $V_{SD} \geq V_{SG} - V_{THP}$ $$I_D = \frac{1}{2} K_P \frac{W}{L}[(V_{SG} - V_{THP})]^2(1 + \lambda V_{SD}) \quad (4.3)$$



(a)



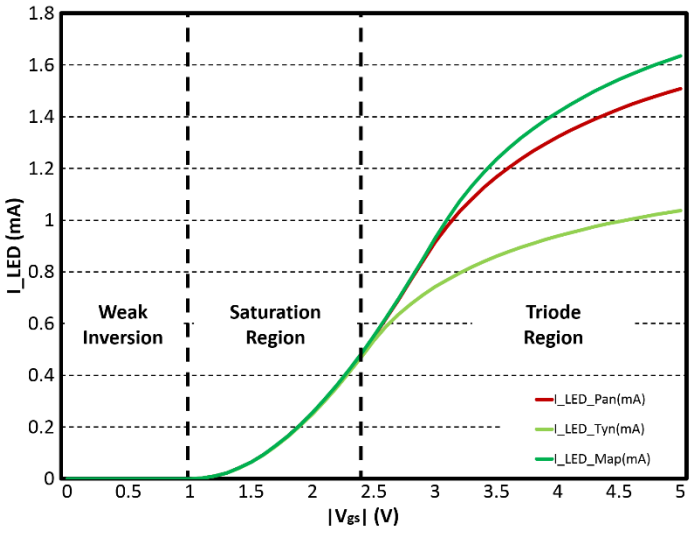
(b)

Figure 4.8 (a) Equivalent circuit of the biphasic drive circuit. (b) Correlation between V_{Drive} and $|V_{gs}|$ (V_{DD}-$V_{Control}$). Based on the equations above, it can be observed that when $|V_{gs}| < 1.0$ V, the drive transistor is in the weak inversion region, and no strong current passes through the LED; when 1.0 V < $|V_{gs}|$ < ~2.3 V, the drive transistor turns into the saturation region; and when $|V_{gs}| > 2.3$ V, the drive transistor operates in the triode region. To note, this chart is using $|V_{gs}|$ as x-axis to analyse the H-Bridge operation status, which is different from the conventional MOSFET I_{DS}-V_{DS} relationship chart.

From Figure 4.8, it is clear that the H-Bridge MOSFETs mostly operate in the triode region rather than the saturation region. When V_{Drive} - $V_{Control} < |V_{th}|$ (MOSFET threshold voltage, ~1.0 V in selected 5 V CMOS process), the drive transistor works in the saturation region, functioning as a current source. However, when V_{Drive} - $V_{Control} > |V_{th}|$, the drive transistor operates into the triode region, and then the drive transistor cannot be considered as a current source. In this situation, the current

through the LED is variable with different I - V characteristics for the different LEDs. And the corresponding I_{LED} - V_{gs}, V_{LED} - V_{gs} and *Liminance* - V_{gs} relationships are simulated and displayed in Figure 4.9.

The reason that the drive transistor mostly operates in the triode region is because the LED requires a relative high maximum voltage drop (3.0 V - 3.6 V). To limit the power consumptions, the maximum power supply is limited to 5 V. This then pushes the drive transistor into the triode operation region. Therefore, although saturation operation has a better current matching performance, the triode operation exhibits much higher efficiency.



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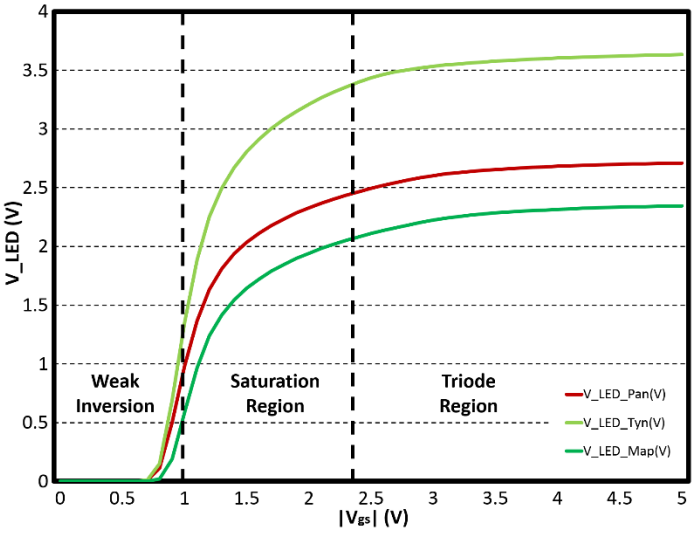

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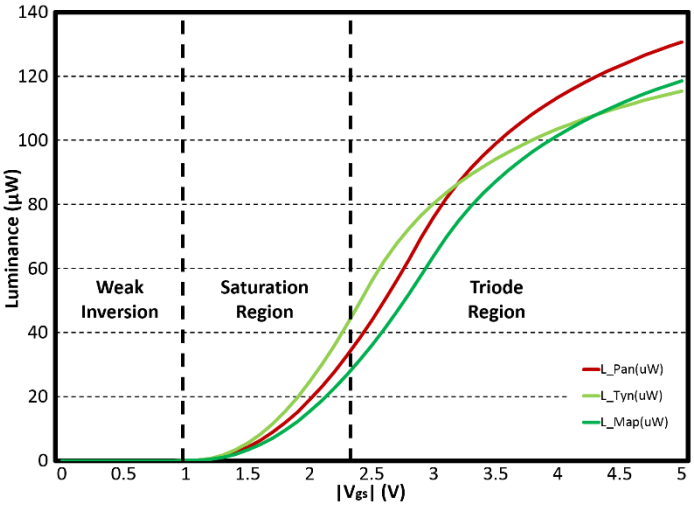


(c)

Figure 4.9 Direct current (DC) analysis of the proposed H-Bridge, simulated with different LEDs when $|V_{gs}|$ is swept from 0 V to 5.0 V (i.e. $V_{Control}$ decreases from 5.0 V to 0 V). (a) The current through the Panasonic, Tyndall, and Maplin LEDs. (b) The voltage across the three different LEDs. (c) Corresponding luminance curves. When V_{DD} is 5.0V, the luminance of all LEDs meet the targeted luminance (≥ 105 µW) of design specifications. Circuit schematic is referred to Figure 4.8 (a).

The simulation results above illustrate that the maximum current range for the different LEDs is in the 1.0 mA - 1.6 mA range, as expected, and the upper limit of the voltage drops are 2.40 V, 2.70 V, and 3.65 V respectively. These values fully meet the requirements stated in Chapter 3, Subsection 3.5.2. Moreover, all the maximum values of LED luminance are over 110 µW, which could lead to the targeted tissue penetrations depth of 300 µm. It indicates that the proposed H-Bridge structure can meet the different needs of all of the selected LEDs. Furthermore, Figure 4.10 shows the Monte-Carlo analysis results of this H-Bridge with the Panasonic µLED. It can be seen that the statistical analysis results for the H-Bridge driving performance are satisfactory. But it is still worthwhile to program and adapt the light driving ability via specific modulation circuitry.

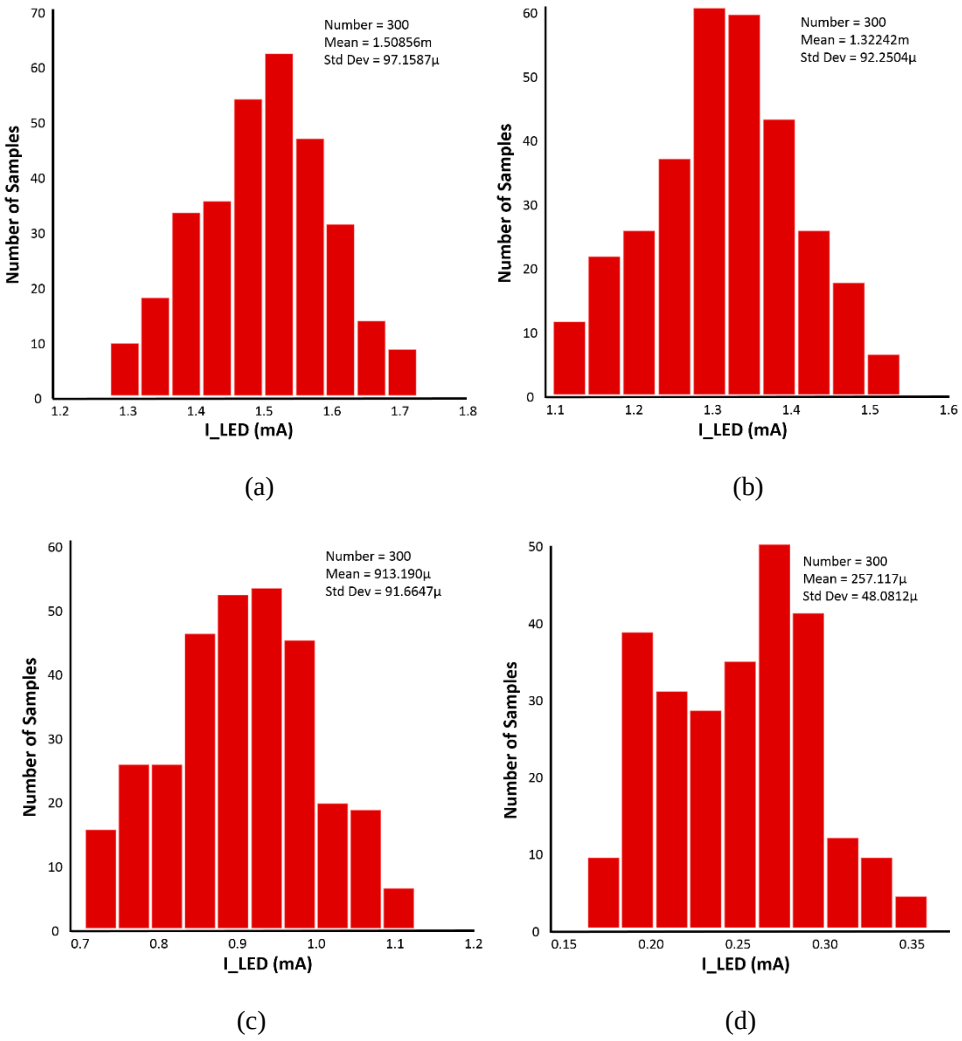


Figure 4.10 Monte-Carlo analysis for I_{LED}. (a) $|V_{gs}|$ = 5.0 V, I_{LED} varies from 1.3 mA to 1.7 mA, and the mean value of I_{LED} is 1.5 mA. (b) $|V_{gs}|$ = 4.0 V, I_{LED} is in 1.1 - 1.55 mA range, with a mean value of 1.32 mA. (c) $|V_{gs}|$ = 3.0 V, I_{LED} fluctuates from 0.7 mA to 1.1 mA, and the mean value is 0.91 mA. (d) $|V_{gs}|$ = 2.0 V, I_{LED} is between 0.18 mA and 0.35 mA, with a mean value of 0.26 mA. Circuit schematic is referred to Figure 4.8 (a).

Monophasic Drive Circuit vs Biphasic Drive Circuit

Although the H-Bridge possesses several advantages, but compared to the monophasic drive circuit, it still has two non-negligible limitations. Firstly, using a same-size drive transistor, the circuit area of the biphasic circuit is 500% larger than the monophasic drive circuit (see Figure 4.11). Moreover, with a same-size drive transistor and the same power supply, the maximum current driving ability of the biphasic circuit is 47.21% lower than that of the monophasic drive circuit (see Figure 4.12). This is due to the complexity of the H-Bridge drive scheme, which has a lower voltage drop across µLED terminals.

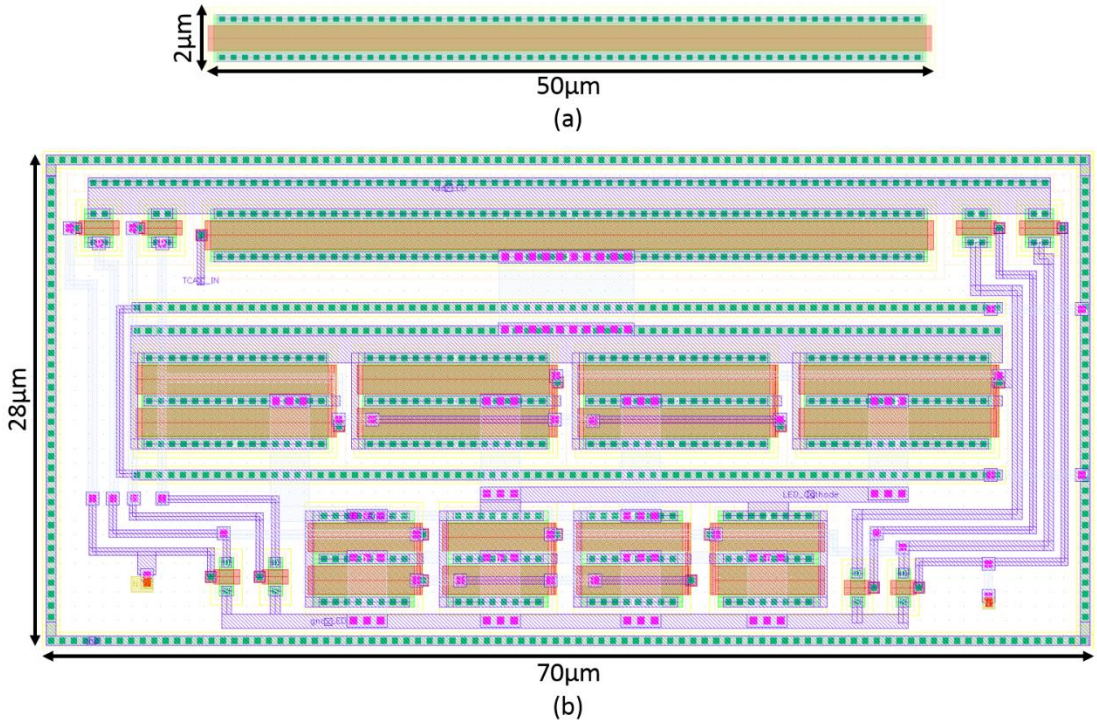


Figure 4.11 Layouts of µLED drive circuitry. (a) Monophasic drive circuit. For comparison purpose, the size of the drive transistor is set to the same size of biphasic drive transistor, 2 µm × 50 µm. (b) Biphasic drive circuit. The circuit dimension is 28 µm × 70 µm.

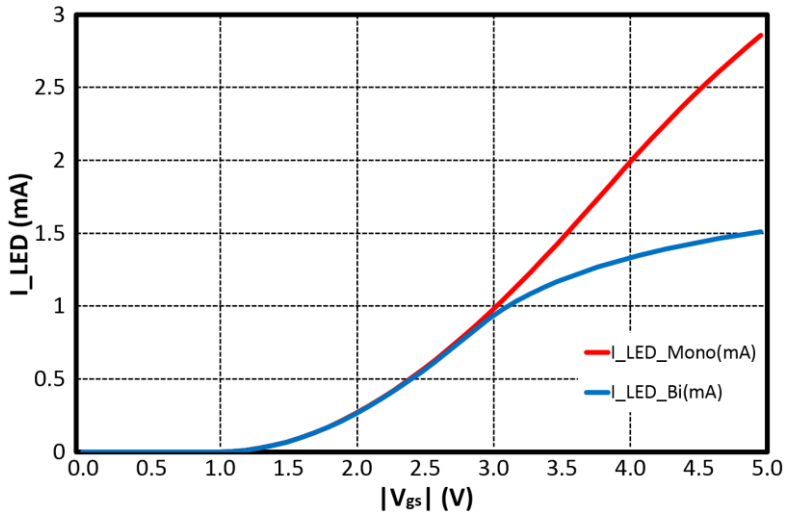
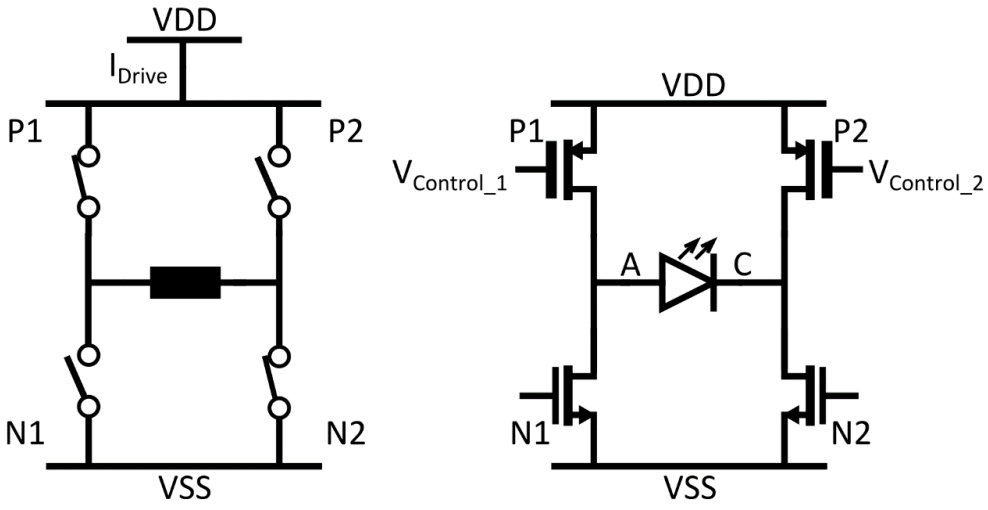


Figure 4.12 Comparison of driving ability between proposed monophasic and biphasic designs. The I_{LED} (max) of the monophasic driver is 2.85 mA while that of the biphasic driver is 1.5 mA. For comparison purpose, the sizes of drive transistors are both set to 50 µm/2 µm.

Updated Biphasic Drive Circuit

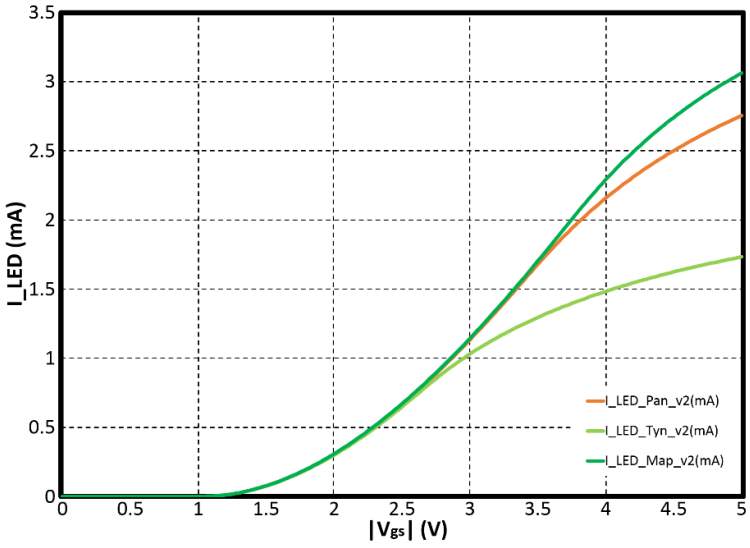
In order to overcome the limitations mentioned above and to improve circuit performance, the H-Bridge structure can be updated as shown in Figure 4.13. In this new design, $V_{Control}$ is directly applied to P_1 and P_2, and the original top drive transistor is removed. Then P_1 and P_2 become new drive transistors and meanwhile

act as switches. In comparison with the circuit in Figure 4.7 (b), this new structure has a better drive voltage range, higher efficiency (see Figure 4.14) and a smaller circuit area of 15 µm × 60 µm, representing a 45% improvement. The only additional cost is the addition of the complexity of logic control, where an analogue DEMUX is required to determine which drive transistor should be activated by $V_{Control}$.

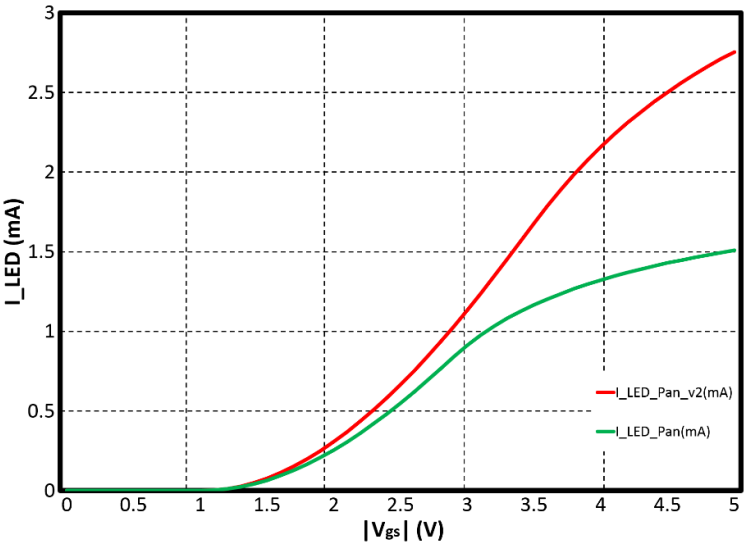


(a) (b)

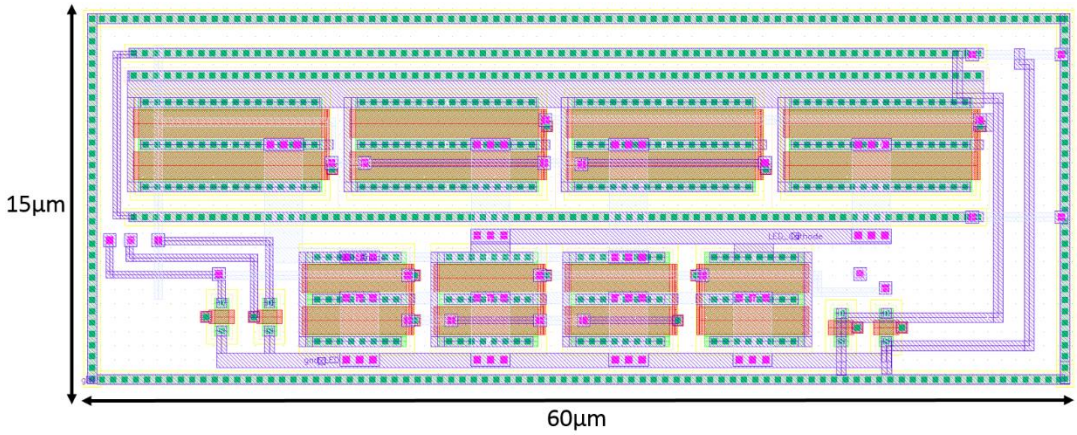
Figure 4.13 H-Bridge_v2. (a) The general diagram of H-Bridge topology. (b) Updated H-Bridge (H-Bridge v2). The original top drive transistor is removed. P_1 and P_2 are two 5 V PMOS transistors, acting as both drive transistors and switches. N_1 and N_2 are two 3.3 V NMOS transistors, acting as switches only.



(a)



(b)



(c)

Figure 4.14 (a) DC analysis of updated H-Bridge, with the current through the Panasonic, Tyndall, and Maplin LED models. (b) Comparison of the driving ability of the two versions of the H-Bridge. (c) Layout of updated H-Bridge structure.

It can be observed from Figure 4.14 (b) that the new H-Bridge has an enhanced maximum µLED driving current from 1.50 mA to 2.75 mA, increasing efficiency by 80%. In the meantime, the circuit area is also reduced. Because of these merits, this updated H-Bridge structure will be implemented in the future design.

4.2.2.4 Summary

This subsection has investigated the µLED drive circuitry, and proposed two types of design: monophasic and biphasic circuits. In particular, two H-Bridge structures have been explored and (will be) implemented into the optrodes. Table 4.2 and Figure 4.15 summarise results of the comparison of the mono-drive circuit, bi-drive circuit (v1) and bi-drive circuit (v2).

Table 4.2 Performance summary of different µLED drivers.

µLED Driver	**PMOS Drive** (Figure 4.3 (c))	**H-Bridge_v1** (Figure 4.7)	**H-Bridge_v2** (Figure 4.13)
Stimulation mode	Monophasic	Biphasic	Biphasic
Current driving range	4.4 mA	1.5 mA	2.75 mA
Luminance range	400 µW	131 µW	235 µW
Circuit area	1 µm × 160 µm	28 µm × 70 µm	15 µm × 60 µm
Transistor quantity	1	5	4

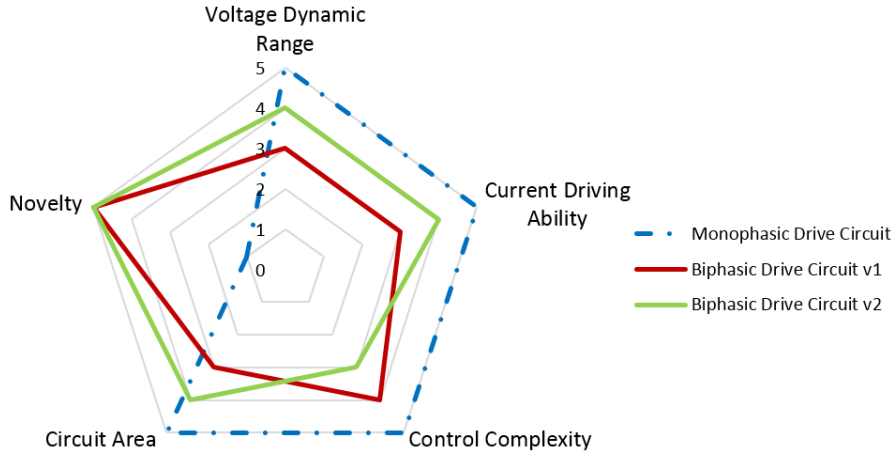


Figure 4.15 Radar diagram compares several main specifications of the µLED drive circuit, including voltage dynamic range, current driving ability, control complexity, circuit area and novelty.

To conclude, compared to the monophasic circuit, although the biphasic circuit has a more complex structure and controlling scheme, it holds significant advantages over the monophasic circuit as highlighted above. In particular, the new H-Bridge design has optimised the trade-off between area, voltage dynamic range, current driving ability and control complexity. This updated H-Bridge design will be applied in future optrode designs.

4.2.3 Intensity Modulation Mechanism

As discussed in Chapter3, Subsection 3.5.2, it is vital to modulate light intensity precisely. Additionally, the influence of the process variations occurring at transistor level has been identified in Subsection 4.2.2 above. This entails distinguished programmability and adaptability of light emissions. Therefore, there is a need for implementing a sophisticated intensity modulation mechanism at circuit level. Here, two modulation schemes are proposed to adjust the light intensity. PWM and intensity magnitude modulation are explained in the following two subsections.

4.2.3.1 Pulse Width Modulation Control

PWM is a modulation technique which utilises digital signals to control different equipment or circuitry. It has been broadly applied in motor control, telecommunications, and power delivery. Here, a PWM method is adapted and simplified to control the µLED drive circuitry. A conceptual diagram is shown in Figure 4.16. The pulse width modulator receives the input data with an enabling signal, and then converts them into output pulses. These output pulses are used to define the stimulation cycles and, consequently, to adjust the light intensity in the time domain. In Section 4.2.4, different types of pulse width modulators are detailed and discussed.

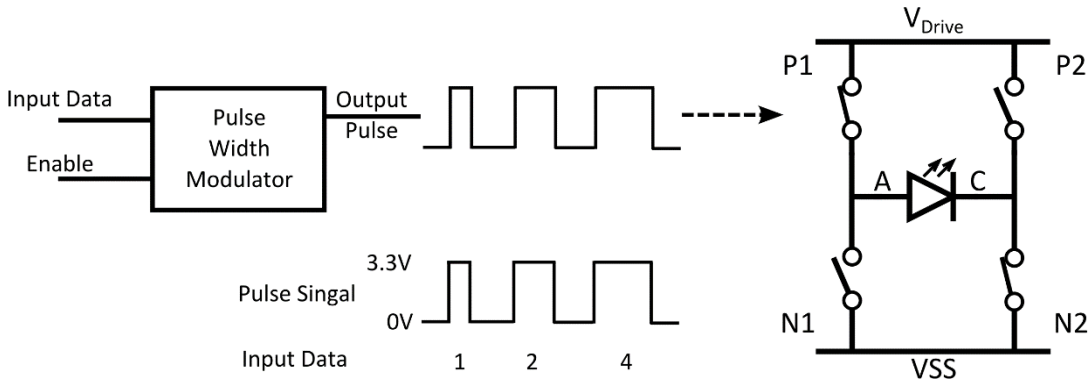


Figure 4.16 Diagram of PWM scheme for the µLED drive circuit. Predefined pulse signals are used to set the stimulation cycle via the control switches.

4.2.3.2 Intensity Magnitude Control

Apart from the timing modulation method discussed above, the light intensity of a µLED is mainly determined by the voltage across the µLED and the current through µLED. When the µLED *I-V* feature is certain, the µLED light intensity is then dominated by the $V_{Control}$ signal of the µLED drivers. If $V_{Control}$ is adjustable, the light intensity can be directly modulated by tuning $V_{Control}$. Here, the intensity magnitude control scheme is illustrated in Figure 4.17. The voltage/current modulator is realised by a DAC (depicted in Subsection 4.2.6) to modulate the $V_{Control}$. An inverting voltage amplifier (as illustrated in Section 4.2.5) is intended to shift the 0 - 3.3 V DAC output to a 5 - 0 V $V_{Control}$ signal. With the adjustment of $V_{Control}$, the µLED current and light intensity can be programmed with predefined resolutions.

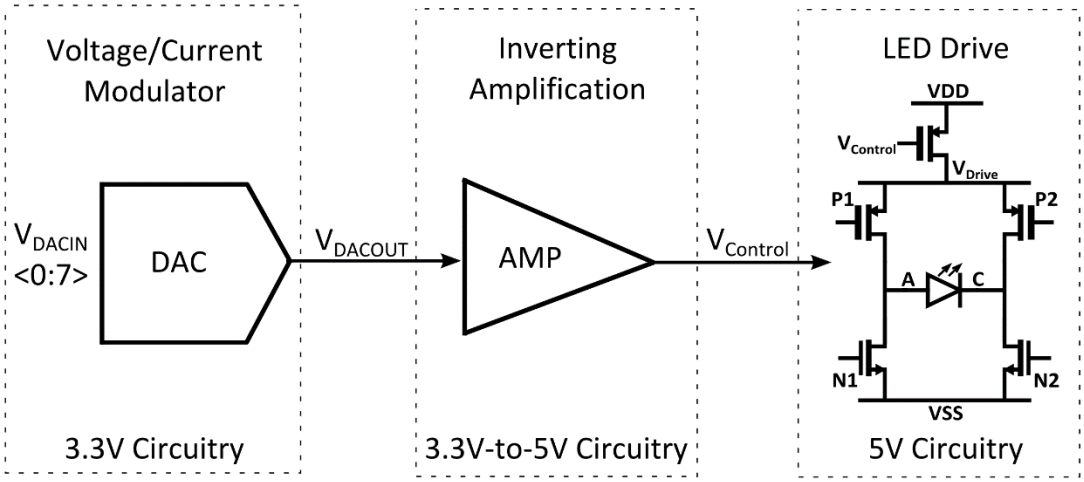


Figure 4.17 Conceptual schematic of proposed intensity magnitude control scheme. DAC is utilised to tune the control voltage of the drive transistor.

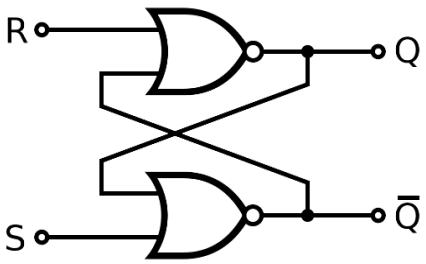
4.2.4 Pulse Width Modulator

In order to pulse µLED operation, the µLED operation status ('*ON*' and '*OFF*') needs to be maintained and updated in real time with particular stimulation cycles. Here, different types of sequential memory units are explored and compared in the following subsections, in order to accomplish and optimise the pulse width modulator design. Three memory units are investigated.

- SR Latch
- D Latch
- SRAM

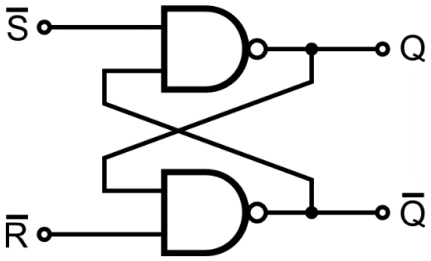
4.2.4.1 SR Latch

Firstly, the S-R (set-rest) latch circuit is presented. There are two types of SR latches: the NOR and NAND versions, as displayed in Figure 4.18. There are two input ports, *S* and *R* (or $\overline{S}$ and $\overline{R}$), and two output terminals, labelled *Q* and $\overline{Q}$, where $\overline{Q}$ is complementary to *Q*.



S	R	Q	Q̄	Operation
0	0	last Q	last Q̄	hold
0	1	0	1	reset
1	0	1	0	set
1	1	0	0	not allowed

(a) (b)



S̄	R̄	Q	Q̄	Operation
0	0	1	1	not allowed
0	1	1	0	set
1	0	0	1	reset
1	1	last Q	last Q̄	hold

(c) (d)

Figure 4.18 SR latch. (a) Circuit design using NOR gates. (b) Function table of the NOR version SR latch. (c) Circuit design using NAND gates (d) Function table of the NAND version SR latch.

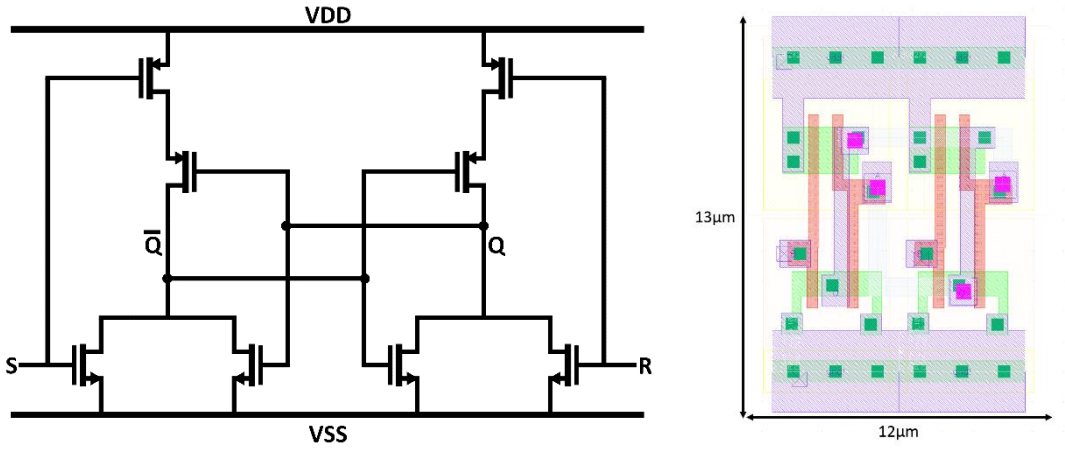
For the NOR version SR latch, when *S* and *R* are both set as '0', the *Q* and $\overline{Q}$ retain the previous state. When *S* is '1' with *R* = '0', *Q* outputs '1'. When *S* is '0' and *R* is '1', then the *Q* is cleared to '0'. When *S* and *R* are stated to '1' simultaneously, the two outputs will both be '0', which is not allowed. The operation of the NAND version SR latch is similar to that of the NOR version, except for two key differences. Firstly, the NAND SR latch is active low; thus the previous state will be maintained only if $\overline{S}$ and $\overline{R}$ are both high. Moreover, when $\overline{S}$ and $\overline{R}$ are activated concurrently, the latch outputs will both be high (which is also undesirable).

During the operation of PWM, the S and R receive the *LED_ON* and *LED_OFF* signals, maintain the µLED operation state and deliver it to the µLED drive circuit. Here, *Q* = '1' is defined to switch on the µLED drive transistor, and *Q* = '0' is set to turn off the particular µLED. If the NAND version SR latch is chosen to build the pulse width modulator, two major issues will arise. First, the NAND version SR latch requires both input signals to be '1' in order to remember the prior state. This will require the external logic control signals to maintain the 'high' state as default, which is not ideal. Although inverters can be utilised to inverse the state, this will increase the design complexity, power consumption and circuit area. Furthermore, when the inputs are both '0', the output of the NAND latch will be forced to '1'. The particular µLED will then be turned on, and an unexpected high current will subsequently be created.

In a regular CMOS design, as NAND gates are preferred over NOR gates, NAND version SR latches are more often chosen than the NOR version [125]. However, for

this particular pulse width modulator design, the NOR version SR latch is a better choice.

A frequency analysis of this NOR version SR latch is conducted. In the post-layout simulation, the maximum frequency of the standalone SR cell is 125 MHz. Then this design is connected to an analogue H-Bridge via a level shifter. In this situation, the maximum switching frequency is recorded as 30 MHz. This indicates that this SR latch can sustain a sufficiently high frequency for light PWM. Besides, the switching energy is also analysed. This design only consumes 63.9 fJ energy per cycle at 1 MHz switching frequency, which is negligible. This SR latch has been selected and implemented in Chapter 5, Section 5.2.3.



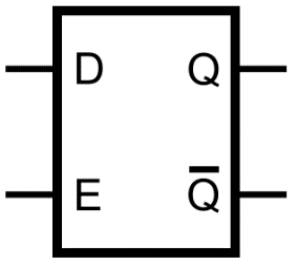
(a) (b)

Figure 4.19 NOR gates-based 8-transistor SR latch. (a) Circuit schematic diagram. (b) The layout diagram. The circuit area is 13 µm × 12 µm.

4.2.4.2 D Latch

The previous subsection has studied the SR latch design, and a NOR version SR latch has utilised to accomplish the pulse width modulator. Although the SR latch proposed above can perform the PWM function, there are still some concerns. First of all, the SR latch has two independent inputs. Thus an additional input port from the global control system is needed, which adds extra logic complexity. Besides, the SR latch would have a precarious metastable state when S and R signals are negated concurrently. If this metastable state occurs, it may lead to incorrect stimulation actions. Additionally, when S and R are activated simultaneously, the operation state of the µLED will be uncertain.

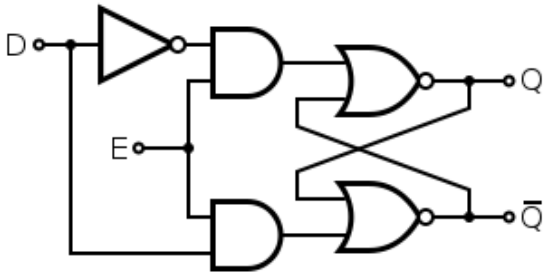
To overcome these limitations, a D latch is proposed and investigated in this subsection. Figure 4.20 shows a schematic diagram of a D latch design. This could be identified as an NOR-based SR latch with an enable signal *E*. Two NAND gates along with an inverter are applied to generate the *S* and *R* functions from a single data input (*D*).



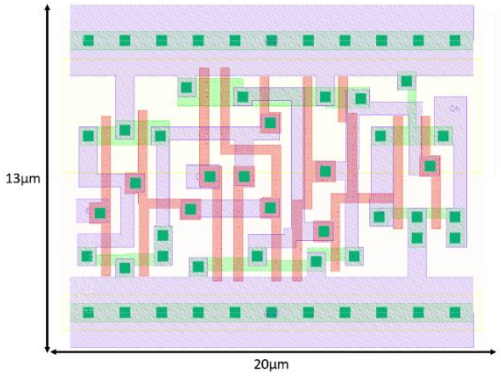
(a)

E	D	Q	Q̄	Operation
1	0	0	1	low
1	1	1	0	high
0	x	last Q	last Q̄	hold

(b)



(c)



(d)

Figure 4.20 SR latch-based 18-transistor D latch design. (a) Logic symbol. (b) Function table. (c) Circuit schematic diagram. (d) Layout diagram, the circuit area is 13 μm × 20 μm..

From the function table shown in Figure 4.20 (b), it can be observed that the *Q* output continuously tracks the *D* input, once the enable signal is triggered. In this situation, the latch can be called ‘open’ state, and the path between *D* input to *Q* output becomes ‘transparent’ (this is the reason for the design being called as *transparent latch*). When the input signal *E* is deactivated, the path from *D* input to the *Q* output is then ‘closed’. Then the *Q* output holds its previous state and stops following the value of *D*, when the *E* signal remains low.

This D latch design converges the previous *S* and *R* signals into a single input signal *D* alongside a flag signal *E*. Through this configuration, the external logic sequences are simplified, the SR metastable hazard is overcome, and the troublesome condition is eradicated when SR are both set to ‘high’ at the same time. With these

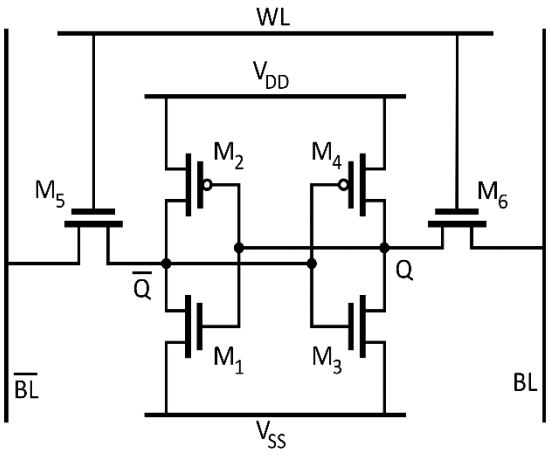
advantages over the SR latch, this D latch has been applied in a new pulse width modulator design and implemented into in Chapter 5, Subsection 5.3.3.

Additionally, based on simulation results, the maximum switching frequency of the standalone design is 100 MHz, and the maximum switching frequency for μLED driver is 25 MHz. Although this is slightly lower than that of the SR latch, it is still perfectly suitable for the system operation requirements. Moreover, it requires 120.6 fJ per cycle switching energy at 1 MHz. This value is 45% higher than that for the SR latch, but it is still within a reasonable energy consumption range.

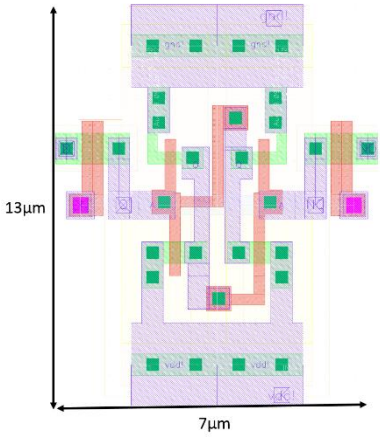
4.2.4.3 SRAM

As discussed above, in comparison with SR latch, the D latch can perform more stable operations with simplified logics. However, the price of gaining these benefits is adding design complexity and increasing the circuit area. In contrast with the 8-transistor SR latch design, the D latch needs 18 transistors, and occupies an additional 67% of chip area for implementation. For this proposed optrode, these limitations are not critical. But in high-density μLED array designs, the space occupation of the D latch may become a blockage when thousands of pulse width modulators are compressed into a compact device.

Thus, in this subsection, the static random-access memory (SRAM) topology is studied for future exploration. A 6-transistor SRAM cell is presented in Figure 4.21. This design consists of two types of functioning cells. The first is the storage cell. Four transistors (M_1, M_2, M_3 and M_4) are formed into a pair of cross-coupled inverters, in which each single bit data (either '0' or '1') is saved. Another cell type is called the access cell. It utilises two transistors (M_5 and M_6) as switches to access the stored data via bit lines (BL and $\overline{BL}$).



(a)



(b)

WL	Q	$\overline{Q}$	BL	$\overline{BL}$
0	0	1	X	X
0	1	0	X	X
1	0	1	0	1
1	1	0	1	0

(c)

WL	BL	$\overline{BL}$	Q	$\overline{Q}$
0	X	X	Q	$\overline{Q}$
1	0	0	X	X
1	0	1	0	1
1	1	0	1	0
1	1	1	X	X

(d)

Figure 4.21 6-transistor SRAM cell. (a) Schematic design, modified from [126]. (b) Layout, the circuit area is 13 μm × 7 μm. (c) Function table when SRAM operates at the read state. (d) Function table when SRAM operates at the write state.

Typically, the SRAM has three working states: holding, reading and writing. Figure 4.21 (c) and (d) shows the function tables of the SRAM cell when it is at the read state and write state, respectively. In the default holding state, when the word line (*WL*) is deactivated, M_5 and M_6 are off, and the storage cells are isolated from the bit line. Consequently, the SRAM cell holds the predefined 1-bit data. In the reading state, the bit lines are pre-charged to high voltage before activating the *WL*. Once the *WL* is triggered, depending on the value of the predefined data, one of the access cells (either M_5 or M_6) will then be discharged. Then the pre-stored value (‘0’ or ‘1’) will be externally sensed and saved. The last mode is the writing operation, which could update new data into the storage cell. At the start, the new data (either the same as or opposite of the pre-stored one) is applied to the bit lines. After that, the *WL* is activated, and the new data is then pushed into the storage cell. In order to overwrite the pre-stored data, the transistors M_5 and M_6 must have higher driveability

than the transistors used in the storage cell. Therefore, in this design, M_5 and M_6 are set to 1 µm/0.7 µm, M_1 and M_3 use minimum size 0.4 µm/0.35 µm, and M_2 and M_4 are with 0.7 µm/0.35 µm.

As the SRAM cell only consumes six transistors, the circuit area is small, and the structure is easy to implement. This design has been employed for initial explorations of an SRAM-based µLED array. In particular, its switching frequency and switching energy are both probed. This SRAM design could sustain at least 10 MHz clock frequency when it is connected to µLED driver, and the maximum value of its standalone switching frequency is 50 MHz. Its switching energy with 1 MHz frequency is only 35.6 fJ per cycle. These parameters are satisfactory both for the proposed optrode implementation and for future designs.

However, even though the SRAM cell has several merits, there are still some concerns. Conventionally, SRAM cells require different types of supporting elements, like write drivers, multiplexers, and read buffers, which results in additional chip area and energy costs. This also increases the workload and complexity of high-level communication systems. Hence, for optogenetic applications, SRAM cells would be mostly employed into a high-density array/matrix modality, which could squeeze the total power and area consumption.

4.2.4.4 Summary

In this subsection, different types of memory units have been investigated, including the SR latch (NOR version and NAND version), D-latch and SRAM cell. Their primary parameters are summarised in Table 4.3.

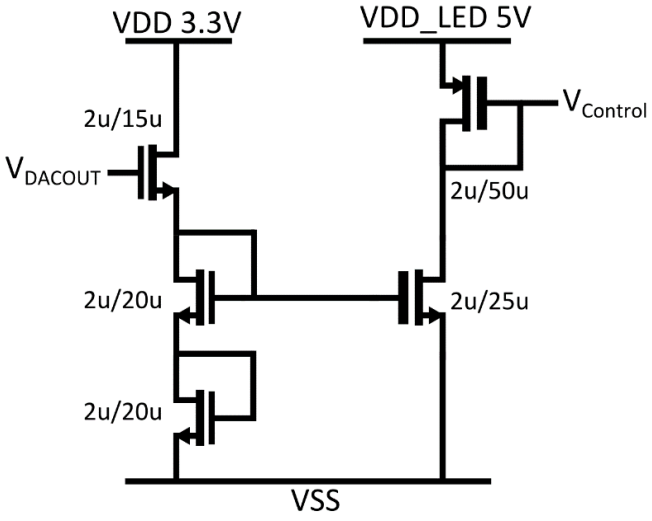
Table 4.3 Main parameters of different pulse width modulators.

	SR Latch	**D Latch**	**SRAM Cell**
Transistor quantity	8	18	6
Operation states	4	2	3
Circuit area	156 μm^2	260 μm^2	81 μm^2
Cell Switching Speed	125 MHz	100 MHz	50 MHz
Driver Switching Speed	30 MHz	25 MHz	10 MHz
Switching Energy	63.9 fJ	120.6 fJ	35.6 fJ

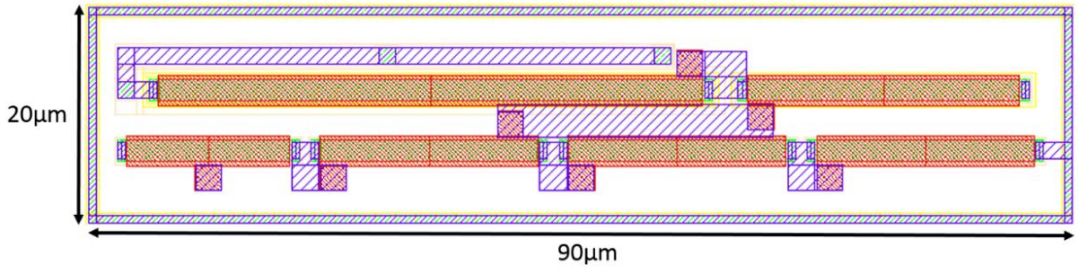
To conclude, all of the proposed pulse width modulators demonstrate various merits. The SR latch could provide the highest switching speed (30 MHz). Its power consumption is also reasonable. Regarding operation stability, however, the SR latch has some limitations, due to the intrinsic metastable states. Also, the SR latch needs two separate input ports, which adds complexity to the global logic control. The SRAM cell represents the simplest topology and occupies the minimum circuit area among all these pulse width modulators. But, this cell needs specific supplementary elements, which increases the total chip area and power consumption. Thus, for optogenetic applications, SRAM cells are more suitable to be constructed into array/matrix patterns for higher-density optical stimulations (such as a retinal prosthesis). The D latch could not only provide stable operations, but can also simplify the high-level logic control. Although the D latch is larger in area, in most CMOS processes it is employed as a standard cell, and this results in less effort to achieve a compact design. Thus, the D latch is an ideal choice of pulse width modulators for this particular optrode.

4.2.5 Inverting Voltage Amplifier

As revealed in Subsection 4.2.3, a DAC module is needed for intensity magnitude modulation. Some DAC designs usually work with 3.3 V operation voltage. But the μLED driver operates at 5 V, and the control voltage $V_{Control}$ of the μLED driver would be decreased from 5 V to 0 V for current adjustments. Thus, there is a need to propose a step-up inverting voltage amplifier (in Figure 4.22) to bridge the 3.3 V DAC module and the 5 V μLED drive circuit.



(a)



(b)

Figure 4.22 A 5-Transistor inverting voltage amplifier. (a) Schematic diagram of the proposed inverting voltage amplifier. It consists of two parts: the diode-connected 3.3 V input stage, and the 5 V inverting output stage. (b) Layout diagram. A guard ring is used to isolate the circuits from digital parts. The block dimensions are only 20 µm × 90 µm.

The proposed amplifier contains two parts: the input stage which functions with 3.3 V power supply, and the 5 V inverting output circuitry. It only consists of five transistors, which can be straightforwardly implemented with minimal area cost. This amplifier achieves two primary functions: 1) signal conversion, it converts the 3.3 V DAC output into a 5 V µLED $V_{Control}$ signal; 2) output range inversion, it inverts the output voltage range in accordance with the PMOS drive transistor.

Performance is verified after connecting the inverting amplifier to the µLED biphasic drive circuit (as shown in Figure 4.7), and then the relationships between $V_{Control}$, I_{LED} and V_{DACOUT} are illustrated in Figure 4.23. It can be seen that, with the change of V_{DACOUT} from 0 V to 3.3 V, the value of $V_{Control}$ decreases from 4.3 V to 0.7 V. When $V_{Control}$ is 0.7 V, the drive transistor is near to fully open, and a high current is then generated. The drive current varies from 0 mA to 1.46 mA. This amplifier cannot achieve the full 0 - 5 V range, so there is a 3% current reduction (the maximum value should be 1.5 mA). But this is negligible for overall µLED driving performance. When the DAC is in the idle state, V_{DACOUT} is 0 V and $V_{Control}$ is 4.3 V. In this situation, although the drive transistor is cut-off, a tiny current may potentially leak through the circuit. Then the drive transistor needs to be connected to the 5 V power supply via an analogue DEMUX, to be entirely shut down.

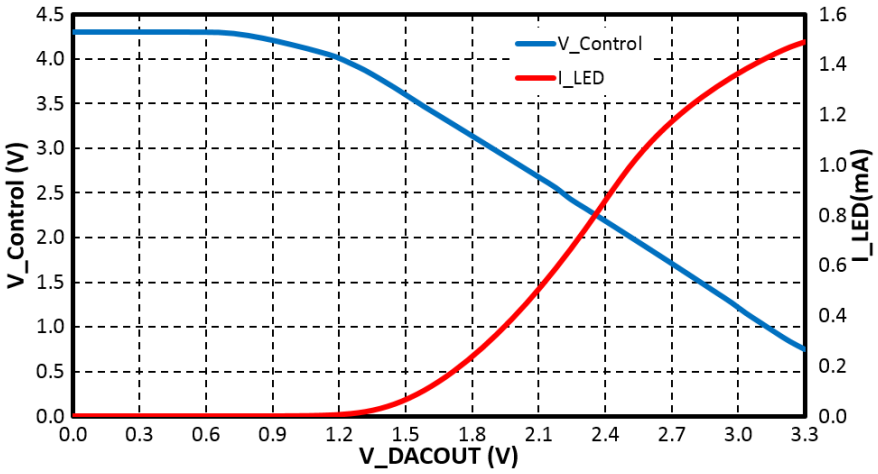


Figure 4.23 Correlations between $V_{Control}$, I_{LED} and V_{DACOUT}. The blue line represents $V_{Control}$, and the red line stands for the I_{LED}. When V_{DACOUT} is gradually tuned from 0 V to 3.3 V, $V_{Control}$ decreases from 4.3 V to 0.7 V, and I_{LED} increases from 0 mA up to 1.46 mA.

Although optical stimulation is performed in the low-frequency region, it is still essential to validate the frequency response of this inverting amplifier. The frequency analysis result is shown in Figure 4.24, indicating that a 135.6 KHz 3 dB bandwidth can be attained, which is sufficient for stimulation operations.

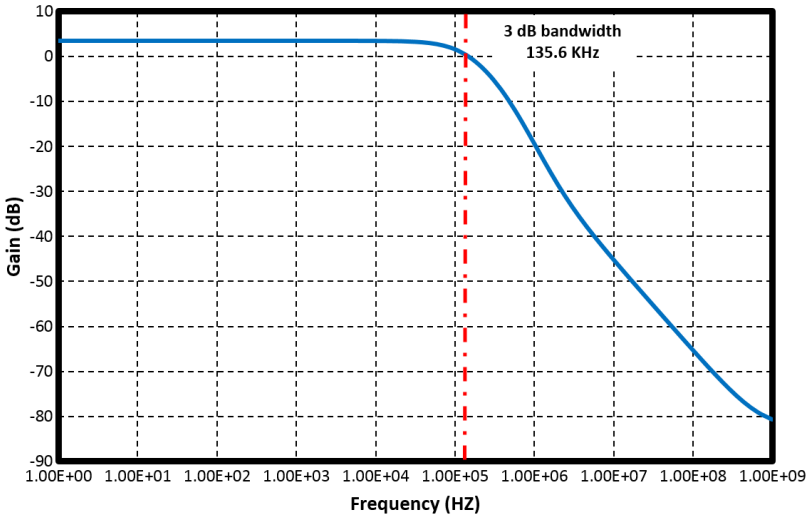


Figure 4.24 Frequency analysis of the inverting voltage amplifier when V_{DACOUT} is 3.3 V. The 3 dB bandwidth of this inverting amplifier is 135.6 KHz.

Power consumption is a constant concern in circuit design. Thus, power analysis is performed for this design as well. It is noted that, when V_{DACOUT} is 3.3 V, the total power consumption reaches the upper limit of 11.5 µW. In particular, the 3.3V circuitry occupies 1.7 µW (0.51 µA×3.3 V), and the 5V circuitry takes up the majority of 9.8 µW (1.96 µA×5 V). Although the total power consumption is reasonable especially for the 5 V circuitry, there is still some space for optimisation.

Power-gating technique and/or feedback topology will be explored in future designs. This 5-transistor inverting voltage amplifier has been implemented in Chapter 5, Subsection 5.3.3, and Table 4.4 summarises the main parameters.

Table 4.4 Main parameters of the inverting voltage amplifier design for stimulation circuitry

Technology	AMS 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V & 5 V
Circuit area	20 µm × 90 µm
Input voltage range	0 - 3.3 V
Output voltage range	0.7 V - 4.3 V
Maximum power consumption	11.5 µW
Bandwidth	135.6 KHz

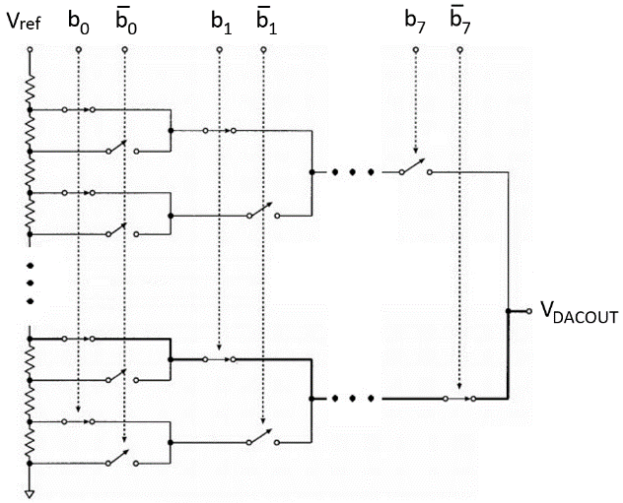
4.2.6 Digital to Analogue Converter

As described above in Subsection 4.2.3, a dedicated DAC module is needed for light intensity adjustment. In Subsection 4.2.5, an inverting voltage amplifier is proposed to bridge the 3.3V DAC module and the 5V µLED driver. Here, the missing part, the DAC module, is introduced. The required DAC design should offer sufficient resolution, occupy a small area and have a reasonable power requirement.

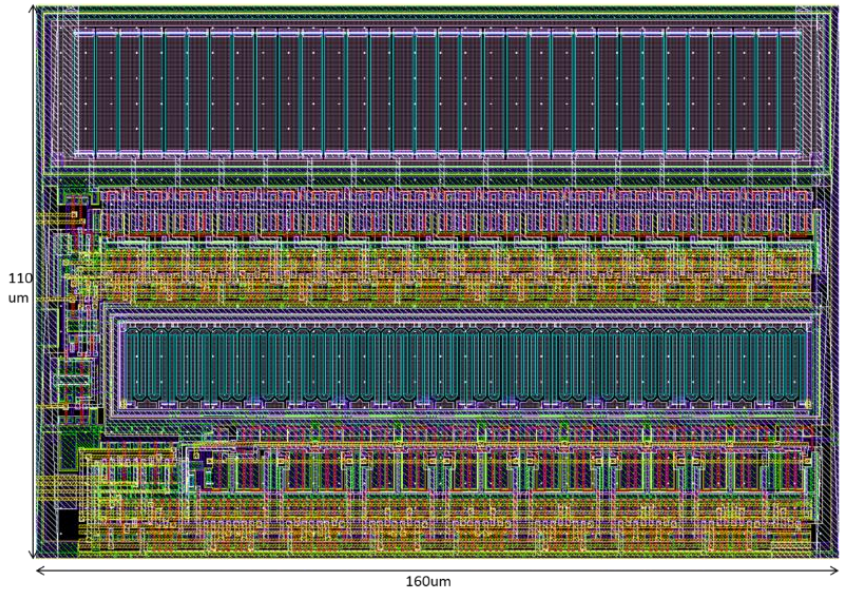
In the following subsections, two types of DACs are presented. Their functionalities are verified, and potential strategies for future improvements are also identified.

4.2.6.1 Resistor String DAC

In general, the most rudimentary DAC would be the resistor string DAC. A simplified schematic of this type of DAC is illustrated in Figure 4.25. It mainly contains a binary switch array and 2^N (N=7 in this particular design) identical resistors. In this architecture, analogue output port (V_{DACOUT}) links with N switches which set as open and another N of them which maintain close, and this can guarantee the conversion speed [127]. This topology can achieve high-resolution data conversion. An off-the-shelf 8-bit resistor ring is adopted from the AMS analogue library [128]. This provides a compact layout, with dimensions of 110 µm×160 µm.



(a)



(b)

Figure 4.25 8-bit resistor string DAC, adopted from the AMS 0.35µm C35B4 process, A_CELLS analogue library [128]. (a) Simplified schematic of this resistor string DAC. It consists of 128 identical resistors and a binary switch array. (b) Layout diagram. The circuit dimensions are 110 µm × 160 µm.

Post-layout simulation is conducted to verify its performance, and the results are illustrated in Figure 4.26. Also, the general parameters are summarised in Table 4.5.

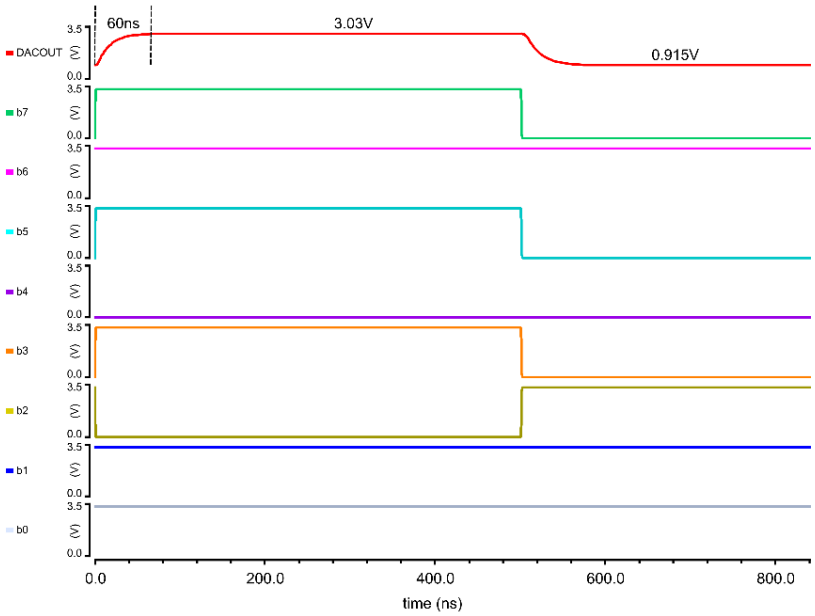


Figure 4.26 Post-layout simulation result of the AMS 8-bit resistor string DAC. Random inputs b<7:0> are set to verify the functionality. The input is changed from <11101011> to <01000111>, and the analogue output is varied from 3.03 V to 0.915 V correspondingly. The output resistance is 21 KΩ. The settling time of this DAC is 60 ns, which is sufficient for stimulation operations. Circuit schematic is referred to Figure 4.25 (a).

Table 4.5 General parameters of the AMS 8-bit resistor string DAC.

Technology	AMS 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V
Resolution	8 bit
Input voltage range	0 - 3.3 V
Differential nonlinearity	±0.25 LSB
Integral nonlinearity	±0.25 LSB
Circuit area	110 µm × 160 µm
Power consumption	260 µW
Output resistance	21 KΩ
Settling time	60 ns

It can be noted that this resistor string DAC has a simple architecture, high resolution, good different & integral nonlinearity, and short settling time. Besides, this DAC design is provided by the AMS C35B4 process with a ready-made layout, which profoundly reduces the development cycle and resources consumption. Therefore, this module has been implemented into Chapter 5, Section 5.3, for both the stimulation circuitry and diagnostic circuitry.

A concern with this design is power consumption. Although the 260 µw power requirement is acceptable for a resistor string DAC, there is considerable room for improvement. A power-gating strategy may be incorporated and, at the same time, it is desirable to investigate other DAC structures.

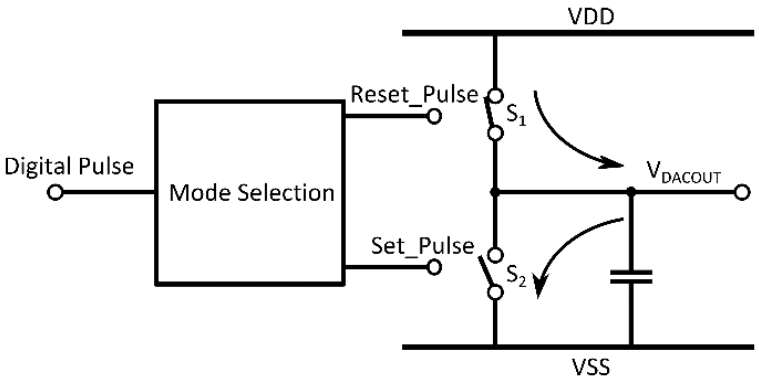
4.2.6.2 Pulse Width Modulated DAC

In the previous subsection, a standard 8-bit resistor string DAC has been introduced and employed into the proposed optrode. Although it has met the need of light intensity control, there are still some points which need to be considered. As highlighted above, the first point is the optimisation of power consumption. Moreover, resistor ring DACs mostly demand S-to-P interfaces (as implemented in Subsection 4.2.7) to receive external serial data, which results in additional energy and area costs. Besides, a large number of resistors are used in this resistor string DAC, and then the total dimensions become relatively bulky. Although this is tolerable for this particular optrode design, it might become a limitation for future more compact and sophisticated devices, such as high-density µLED arrays for visual prostheses.

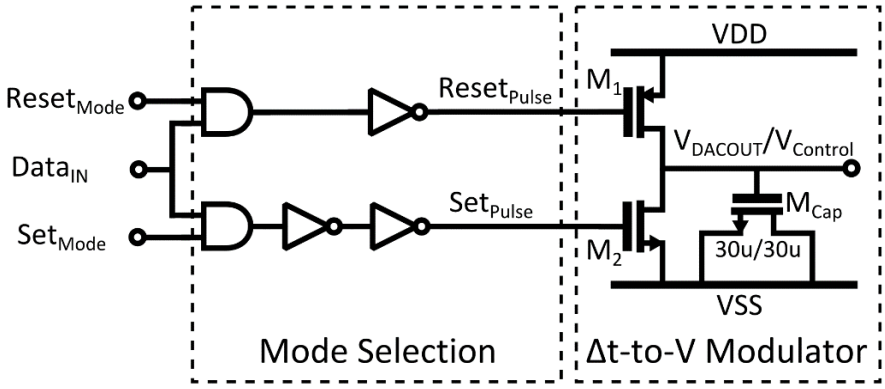
Hence, it is meaningful to study alternative DAC design methodologies which can be beneficial both for the current optrode implementation and future explorations. Here, a pulse width modulated DAC is investigated. This pulse width modulated DAC is based on an adapted switch-capacitor topology, as shown in Figure 4.27 (a). This pulse modulated DAC requires only one digital input signal, and this signal contains the predefined pulse width information. The pulse signal is then combined with a mode selection signal (either *Reset_Pulse* or *Set_Pulse*) to determine the operation mode. If enabling the reset mode, the S_1 will be closed and S_2 will be kept open, and then a charge current would drop from V_{DD} to the capacitor. Consequently, V_{DACOUT} will be charged up to V_{DD}. If the set mode is selected, S_1 will be in the open state and V_{DD} is isolated from the capacitor. At the same time, the S_2 path will be clear, and V_{DACOUT} will be gradually discharged until the *Set_Pulse* is terminated or V_{DACOUT} is equal to V_{SS}. Using this strategy, the value of V_{DACOUT} could be modulated from 0 V to V_{DD} (3.3 V or 5 V), corresponding with the input pulse width.

Figure 4.27 (b) shows the circuit schematic of this pulse width modulated DAC. It mainly consists of two modules: a mode selection module and a time to voltage

modulator. In the mode selection module, two AND gates are used to mingle the input pulse with the reset and set signals separately. After that, inverters are put into the path, buffering the input signals. In the time to voltage modulator part, a PMOS (M_1) with the minimum size of 0.4 µm/0.5 µm acts as a switch to rapidly recharge the V_{DACOUT} back to V_{DD}. Meanwhile, a long NMOS (M_2, 1 µm/25 µm) is chosen as S_2 to steadily adjust/discharge the V_{DACOUT}, until reaching the expected voltage. In order to achieve a reasonable conversion resolution, the discharge operation cannot be over-fast. That is the reason why the width/length ratio of M_2 is comparatively small.



(a)



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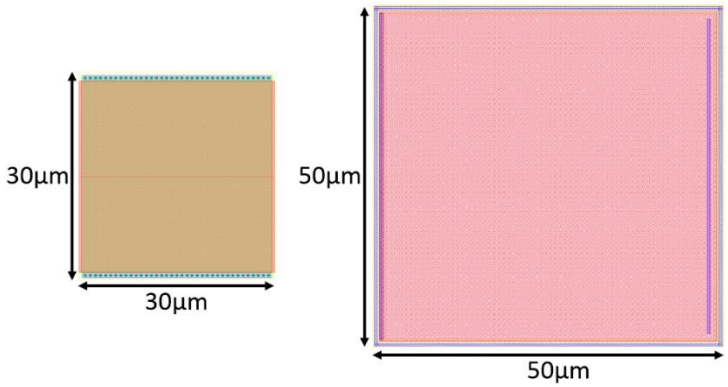

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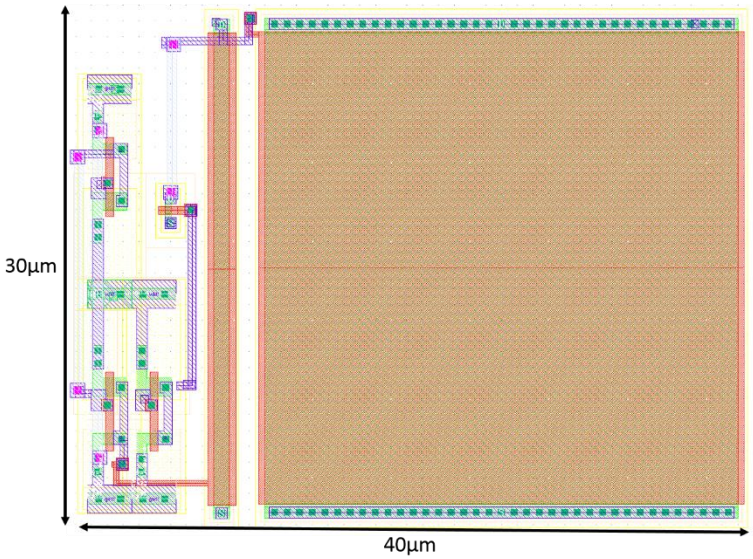


(d)

Figure 4.27 The proposed pulse width modulated DAC. (a) Conceptual diagram. This DAC is based on an adapted switch-capacitor topology. (b) Schematic design of this DAC, using 5 V transistors. (c) Area comparison of MOSFET-based capacitor and conventional poly-to-poly capacitor. (d) Layout of the pulse width modulated DAC. The circuit dimensions are only 30 µm × 40 µm.

For the choice of capacitor, instead of using a conventional poly-to-poly capacitor, a NMOS (M_{Cap}) is utilised to function as a capacitor. The primary reason for this is the poly-to-poly mask was not chosen for the X-Fab wafer fabrication, which reduced the money cost. For this particular capacitor design, all of terminals of M_{Cap} are grounded together except the Gate terminal, and the capacitance value is the total capacitance C_{ox} between the gate terminal and the source/drain terminals [127]. Compared to the poly-poly capacitor, the MOSFET-based capacitor needs less chip area. As shown in Figure 4.27 (b), the dimensions of M_{Cap} are 30 µm×30 µm. By checking the characterisation value of C'_{ox} (4.54 fF/µm^2) from [129] and applying the equation $C_{ox} = C'_{ox} \times W \times L$, the capacitance of M_{Cap} is calculated as 4.0 pF. In contrast, if choosing a conventional capacitor design, such as a poly-poly capacitor in AMS 0.35µm C35B4 process, with the same value of capacitance, the circuit area will be 50 µm×50 µm.

The leakage effect of this MOSFET-based capacitor is analysed, and the leakage current is in the fA range. This amount of leakage current is appropriate for both stimulation circuitry and diagnostic circuitry, since all the optrode operations are in the range of milliseconds or seconds. But if this pulse width modulated DAC is applied in some long-term operation scenarios, the leakage effect might become a

concern. In that case, the conventional capacitor would be a safer choice, although it will increase the area consumption.

Having introduced the design approaches above, a post-layout simulation is conducted to validate its performance, and the results are depicted in Figure 4.28. Firstly, the reset mode is asserted with a fixed value of 1 µs. It maintains the default voltage value (5 V) of the capacitor. At this time, the reset transistor M_1 is on and the set transistor M_2 remains off. After deactivating the reset mode, the V_{DACOUT} still maintains the 5 V voltage, and M_1 and M_2 are both off until the predefined *Set_Pulse* is pushed in. When the *Set_Pulse* signal is applied to M_2, the V_{DACOUT} gradually decreases until the *Set_Pulse* is negated or V_{DACOUT} is equal to 0 V. Then, the V_{DACOUT} retains the updated value. By repeating this *Reset-Set* loop, the V_{DACOUT} could then be configured in real-time for light intensity adjustments.

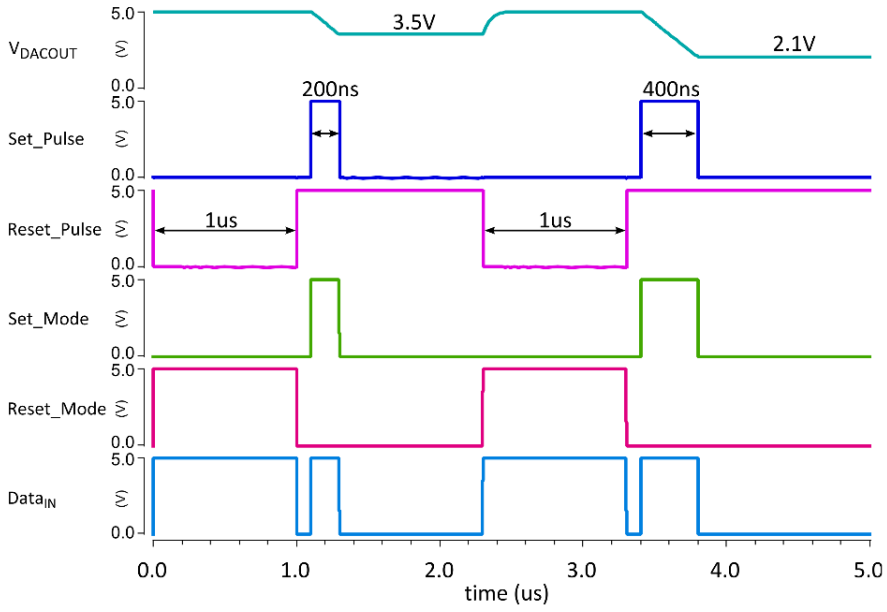


Figure 4.28 Post-layout simulation results of the proposed pulse modulated DAC. The reset pulse signal is set to a fixed value, 1 µs, and it can be shrunk to 300 ns in practical use. The minimum dead time between *Set_Pulse* and *Reset_Pulse* is equal to one clock cycle. The set pulse signal is randomly chosen as 200 ns and 400 ns, and 3.5 V and 2.1 V analogue outputs are then retained correspondingly. Circuit schematic is referred to Figure 4.27 (b).

Tracing the simulation above, to sweep the *Set_Pulse* from 0 ns with a predefined *Reset_Pulse* value, the correlation between the *Set_Pulse* and the V_{DACOUT} could then be deduced, as illustrated in Figure 4.29. Initially, when the *Set_Pulse* is deactivated, the V_{DACOUT} is set to 5 V. And then V_{DACOUT} linearly decreases to 0 V when the *Set_Pulse* is steadily adjusted to 800 ns. A suitable linearity is demonstrated between

V_{DACOUT} and *Set_Pulse*. The performance of this DAC is also investigated when it operates with a 3.3 V power supply. Then, it can be found that the DAC requires a longer *Set_Pulse* cycle to sweep the V_{DACOUT} value, and this is because the *Reset-Set* (charge-discharge) loop is running slower with a lower power supply. The default operation frequency is set to 10 MHz, which could obtain 8 sampling points with 5 V power supply and 13 sampling points with 3.3 V power supply. More sampling points can be achieved when increasing the frequency. In actual use, the maximum operation frequency is determined by the external controller (field-programmable gate array, FPGA), i.e. 100 MHz in this work. Then the maximum sampling points would be 80 (5 V) and 130 (3.3V) respectively.

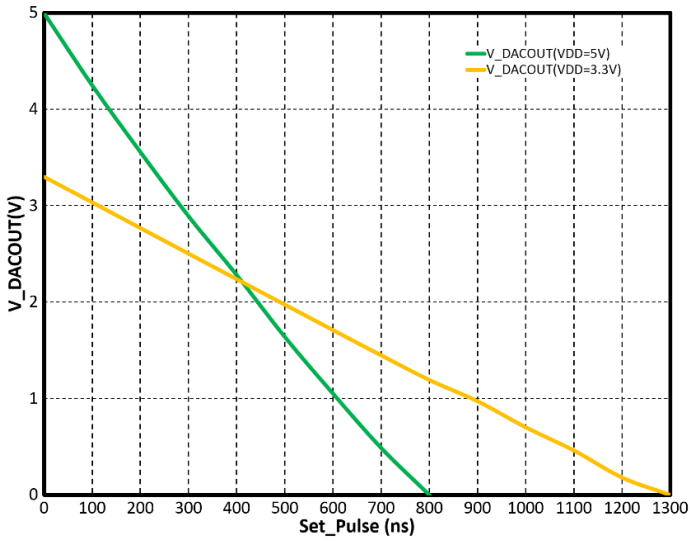


Figure 4.29 Relationship between *Set_Pulse* and V_{DACOUT}. When V_{DD} is 5 V, V_{DACOUT} is gradually decreased from 5 V to 0 V when *Set_Pulse* is swept from 0 ns to 800 ns. When V_{DD} is reduced to 3.3 V, the maximum value of *Set_Pulse* is increased to 1300 ns.

Moreover, a power analysis is also executed. Here, each *Reset-Set* loop is defined as a 'sequence', and the transient power consumption during each sequence is analysed. Then, the energy consumption of each sequence is obtained by integrating the transient power, and the results are shown in Figure 4.30. When V_{DD} is 5 V, the energy consumption per sequence increases from 6.2 pJ to 24.3 pJ when the *Set_Pulse* signal varies from 0 ns to 800 ns. And the average power consumption is calculated as 8.45 µW. In contrast, 3.3 V operation has a lower energy requirement. The energy consumption per sequence is changed from 2.6 pJ to 10.3 pJ while sweeping *Set_Pulse* from 0 ns to 1300 ns, with a 3.34 µW power consumption on

average. Therefore, this pulse modulated DAC demonstrates fairly low energy dissipation both with 3.3 V and 5 V power sources.

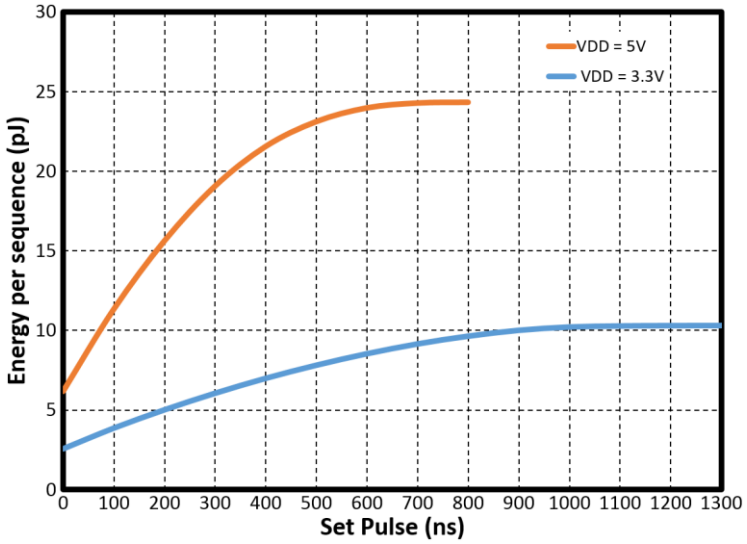


Figure 4.30 Energy consumption analysis per sequence. V_{DD} is set to 5 V and 3.3 V separately. The *Reset_Pulse* is still with the 1 µs setting, and *Set_Pulse* signals are tuned in the 0 - 800 ns and 0 - 1300 ns ranges respectively. The maximum energy consumption per sequence is below 25 pJ. If needed, further reduction can be obtained by trimming the *Reset_Pulse* to 300 ns (the minimum charging time for M_{Cap}).

Apart from its simple design and low energy consumption, this pulse modulated DAC has other additional superiorities. Firstly, thanks to its single digital input, S-to-P conversion becomes unnecessary, which simplifies the system design and avoids extra power and space costs. Secondly, the converter output voltage range exactly matches with the µLED drive voltage $V_{Control}$, i.e. from 5 V to 0 V. Thus this pulse modulated DAC can be directly applied to the µLED drive transistor to tune the $V_{Control.}$ In other words, the DAC output V_{DACOUT} is playing the role of $V_{Control}$ (which is the reason why the DAC output is referred to $V_{DACOUT}/V_{Control}$ in Figure 4.27 (b)). Owing to this delightful feature, the necessity for the Inverting Voltage Amplifier (proposed in Subsection 4.2.5) could be avoided, and this results in a further reduction in energy and area consumption. Because of these merits as elaborated above, this DAC has been implemented in Chapter 5, Subsection 5.2.4. The overall performance of the pulse modulated DAC is summarised in Table 4.6.

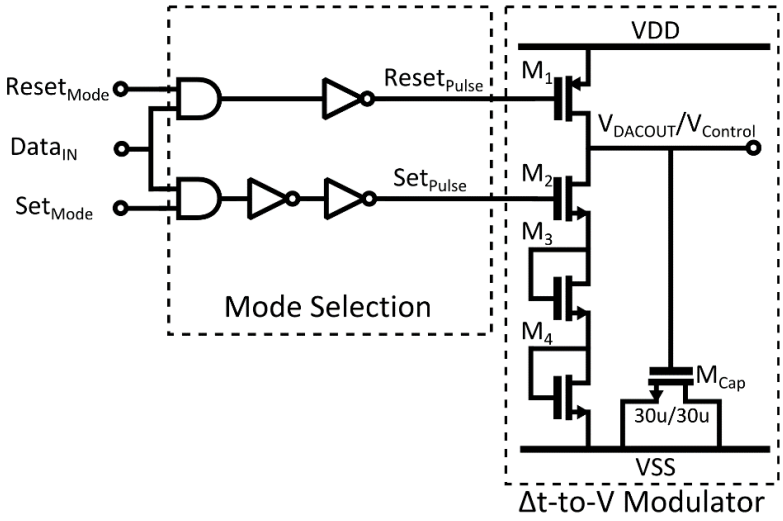
Table 4.6 Main parameters of the pulse modulated DAC.

Technology	X-FAB 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V/5 V
Sampling Points	130/80
Dynamic Range	43 dB/38 dB
Input voltage range	0 - 3.3 V/5 V
Output voltage range	0 - 3.3 V/5 V
Circuit area	30 µm×40 µm
Static power consumption	3.7 fW/5.77 fW
Dynamic power consumption	3.34 µW/8.45 µW
Energy per sequence	(max) 10.3 pJ/24.3 pJ
Clock Frequency	10-100 MHz

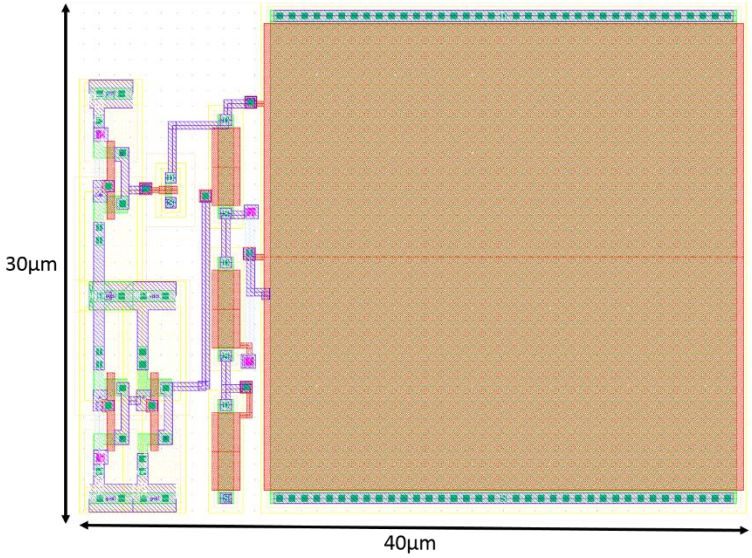
4.2.6.3 Updated Pulse Width Modulated DAC

The previous subsection has presented a capacitor based pulse modulated DAC design. Owing to its small dimension and minimal energy costs, it has been implemented into each local channel of the diagnostic sensing subsystem in Chapter 5. However, there are still some concerns which need to be considered. It can be seen from Figure 4.29 above, this DAC design requires (at least) 10 MHz to set the pulse signals and generate specific sampling points, and this is achievable for this particular optrode design. But if aiming to adopt this DAC design into lower frequency applications or to provide more sampling points, its comparatively high operation frequency would be a limitation.

Thus, in this subsection, an updated pulse modulated DAC is proposed, for which the schematic diagram is demonstrated in Figure 4.31. In this updated design, a serial stage (M_2, M_3, and M_4) is created. The dimensions of each element (both analogue and digital) are the same as those in the original version described in the previous subsection, except that M_2 is shrunk to 1 µm/5 µm and M_3 & M_4 retain the same settings as M_2. The updated layout is also displayed in Figure 4.31. It can be seen that, although this serial stage needs two more transistors, the overall circuitry dimensions are still the same as the original version.



(a)



(b)

Figure 4.31 Updated pulse width modulated DAC. (a) Updated schematic diagram. A 2-transistor serial stage is added into the original DAC design. (b) Layout of this updated pulse width modulated DAC. M_2, M_3 and M_4 are all defined as 1 µm/5 µm, maintaining a miniature structure. The circuit dimensions are still kept as 30 µm × 40 µm.

By adding this serial stage, the discharging speed of the capacitor would be slowed down, which results in a much higher conversion resolution. The simulation results are depicted in Figure 4.32. When this DAC is powered by a 5 V supply voltage, it could provide 0.03 V conversion resolution with 10 MHz frequency, and the number of sampling points could be tenfold increased. If keeping the original quantity of sampling points, the required operational frequency could be less than 1 MHz, which would be suitable for lower-frequency operation. And the power consumption is even lower than the original design, with an average value of 4.8 µW.

When this updated DAC is operated at 3.3 V, it the conversion resolution could be further increased, as the *Reset-Set* (charge-discharge) loop would be longer with lower power supply. Also the power would be further reduced, with 2.1 µW on average.

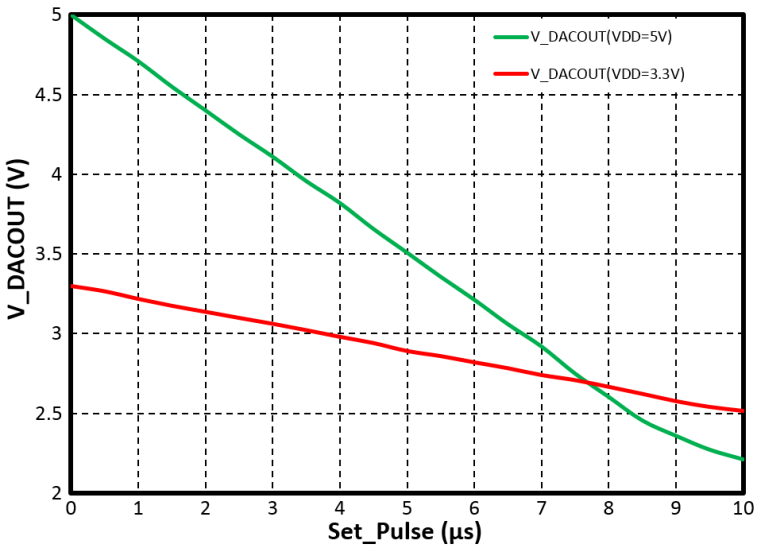


Figure 4.32 Linearity of the updated pulse width modulated DAC. When V_{DD} is 5 V, V_{DACOUT} is gradually decreased from 5 V to 2.3 V when the *Set_Pulse* is swept from 0 µs to 9 µs. When the *Set_Pulse* is longer than 9 µs, the pulse-voltage conversion becomes nonlinear. When V_{DD} is reduced to 3.3 V, with the same *Set_Pulse* signals, the V_{DACOUT} varies from 3.3 V to 2.5 V, demonstrating a satisfactory linearity.

The only concern with this updated pulse modulated DAC design is its limited linear working range. It can be seen from the green curve in Figure 4.32 that, when the *Set_Pulse* is gradually increased from 0 µs to 9 µs, the V_{DACOUT} is steadily discharged from 5 V to 2.3 V. Then, in the 9-10 µs region, the V_{DACOUT} is decreased to 2.2 V; however, the conversion becomes nonlinear. This is because the serial stage is working at (or near) the weak inversion region when V_{DACOUT} is lower than 2.3 V. This nonlinearity feature is tolerable for this particular optrode operation, but it might be a limitation for other applications.

Instead of incorporating this 2-transistor serial stage, another solution to decrease the operation frequency and improve sampling resolution would be to simply expand the dimensions of the capacitor and the length of M_2. But this will incur higher area costs, which is not ideal for this particular implantable application and then not detailed here.

Table 4.7 General parameters of the updated pulse modulated DAC.

Technology	AMS 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V/5 V
Sampling Points	1000
Dynamic Range	60 dB
Input voltage range	0-3.3 V/5 V
Output voltage range	2.5-3.3 V/2.3-5 V
Circuit area	30 µm×40 µm
Static power consumption	0.7 fW /1.49 fW
Dynamic power consumption	2.1 µW/4.8 µW
Clock Frequency	1-100 MHz

4.2.6.4 Summary

In this subsection, the resistor string topology and the PWM mechanism are both explored for DAC designs. These two types of DACs have been implemented into optrodes, and their overall performances are summarised and compared in Table 4.8. The resistor string DAC can provide comparatively high conversion resolution. But it requires high power consumption, and this would be a bottleneck for implantable applications. Besides this, although the layout of the resistor string DAC is compact, the circuit area is still bulky. Additionally, it requires a dedicated S-to-P interface and supplementary logic cells, which adds workload for circuit design and increases the complexity of logic control. Compared to the resistor string DAC, the two versions of pulse modulated DAC demand significantly low area and power consumption. They also avoid the need for amplification/inversion stages and a S-to-P interface. But some limitations have also been identified. The first pulse modulated DAC requires a comparatively high operation frequency (≥10 MHz) to achieve particular specific sampling points. Although this is suitable for the requirements of the proposed optrode design, it might not be suitable for some other lower-frequency applications. The updated version can provide higher conversion resolution with lower operation frequency, but it has a narrower linear working range. Even though it is again acceptable for this particular optrode operation, it would not be ideal for wider applications. Diverse design and optimisation strategies (such as a current steering DAC) need to be explored in the future to improve the DAC performance.

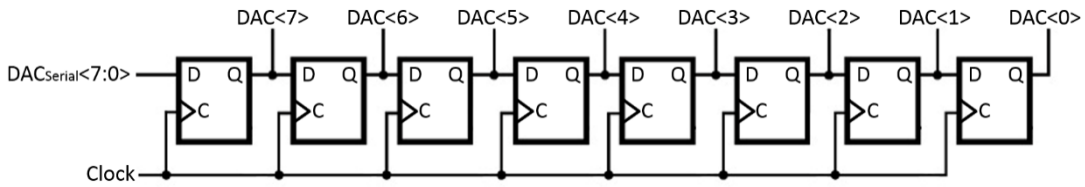
Table 4.8 Performance comparison of three DAC designs.

DAC	Resistor String	Pulse Modulated	Pulse Modulated_v2
Technology	AMS 0.35-µm, 2P4M CMOS	X-FAB 0.35-µm, 2P4M CMOS	AMS 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V	3.3 V/5 V	3.3 V/5 V
Sampling Points	256	130/80	1000
Dynamic Range	48 dB	43 dB/38 dB	60 dB
Input voltage range	0 - 3.3 V	0 - 3.3 V/5 V	0 - 3.3 V/5 V
Output voltage range	0 - 3.3 V	0 - 3.3 V/5 V	2.5-3.3 V/2.3-5 V
Circuit area	110 µm×160 µm	30 µm×40 µm	30 µm×40 µm
Power Consumption	260 µW	3.34 µW/8.45 µW	2.1 µW/4.8 µW

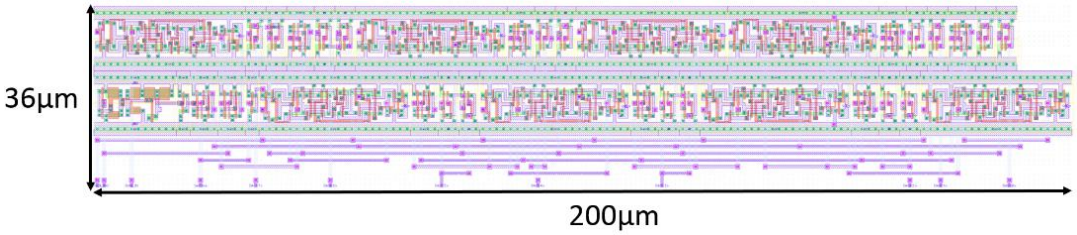
4.2.7 Serial to Parallel Interface

As mentioned in Subsection 4.2.6.1, for a conventional multi-input DAC, a S-to-P interface needs to be included. Thus, this subsection details the design and implementation of an 8-bit S-to-P interface which is used for the resistor string DAC.

Figure 4.33 shows the simplified structure of the serial-in, parallel-out converter. It mainly contains a series of D flip-flops. The input signal DAC_{Serial} <7:0> is the predefined 8-bit data string, and the outputs are all of the stored DAC bits. Accessory logic cells are added into the S-to-P for timing control, and due to their simplicity these cells are not depicted in detail.



(a)



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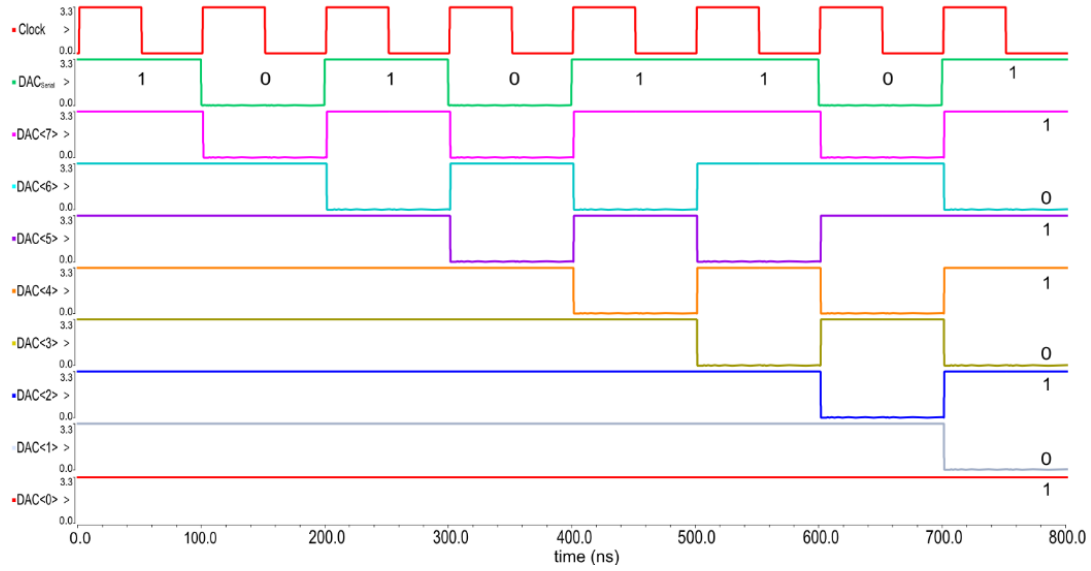
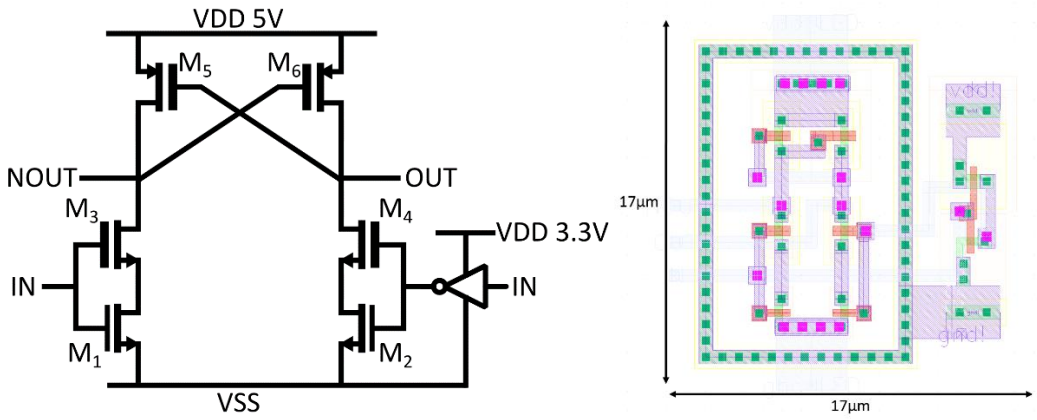


(c)

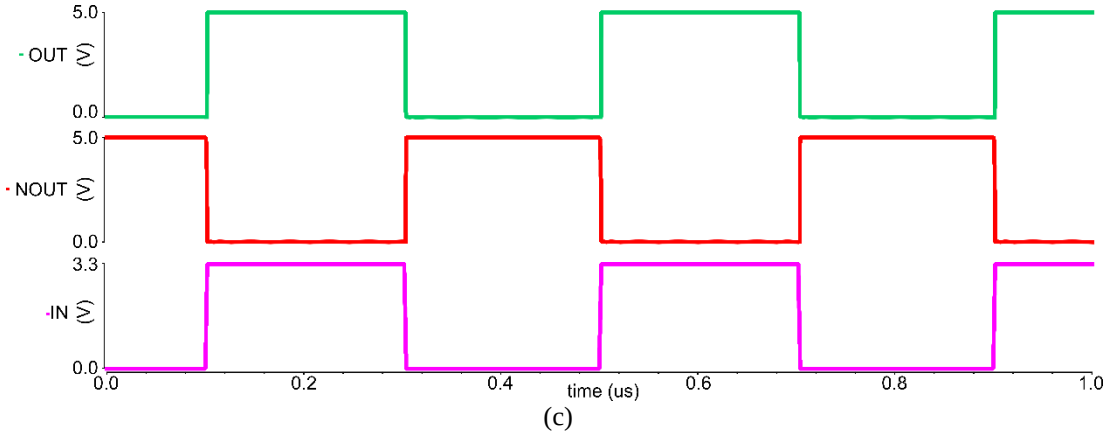
Figure 4.33 (a) Simplified schematic of the S-to-P interface. (b) Layout of the S-to-P interface, including accessory logic cells. The circuit dimensions are only 36 µm × 200 µm. (c) Simulation results of S-to-P conversion. A random input data string is chosen as {10101101}. At the last clock cycle, the conversion is finished, and 8-bit parallel outputs are latched for DAC usage.

4.2.8 Level Shifter

As illustrated in previous sections, the µLED drive circuit works at 5 V to obtain a high voltage drop across the µLED. However, most of the digital cells used in the proposed optrode are in the standard 3.3 V, which could save area and power costs, and they are also compatible with external test benches (both microcontroller and FPGA). Here, in order to bridge the 3.3 V digital elements with the 5 V µLED drive circuit, a 3.3 V-to-5 V up-converting level shifter is briefly introduced, and its schematic, simulation and layout are all shown in Figure 4.34. This level shifter has been implemented into Chapter 5, Subsection 5.3.3.



(a) (b)



(c)

Figure 4.34 Proposed 3.3 V-to-5 V up converting level shifter. (a) Schematic design. M_1, M_2 and the inverter are with a 3.3 V power supply, and M_3, M_4, M_5 and M_6 use 5 V MOSFETs. All the transistors are set with minimum size. (b) Layout diagram. A guard ring is utilised to remove substrate noises caused by digital switching. (c) Transient simulation results.

4.2.9 Summary

This section has firstly introduced the general system architecture of the optical stimulation circuitry. After that, the design and implementation of each principal component has been individually detailed. Monophasic and biphasic µLED drivers have both been developed to generate the expected high current for light emission. Then both PWM and intensity magnitude modulation methods have been investigated, to obtain excellent light intensity controllability. Three types of pulse width modulators have been proposed, analysed and compared, and they have been employed into specific optrode developments. Afterwards, a dedicated step-up Inverting Voltage Amplifier has been created to link the conventional 3.3 V circuitry with the 5 V µLED drive circuitry. Following that, two types (and three versions) of DAC modules have been proposed and utilised for stimulation function and/or diagnostic function. Additionally, an accessory S-to-P interface and level shifter have been constructed to complete the system design.

All of the circuits described in this section have been implemented into different optrode designs in Chapter 5, to form both the optical stimulation circuitry and diagnostic sensing circuitry. In the following section, dedicated diagnostic sensing circuits are designed and implemented.

4.3 Diagnostic Sensing Circuitry

4.3.1 Introduction

Since the optrode (including the µLEDs) is intended to be implanted into brain tissue, the system stability is a key concern for long-term continuous operation. One hazard is that optrode breakage may happen during or post implantation. Another consideration concerns the operational degradation of the light emitters. In particular, contact corrosion between the µLEDs and the CMOS circuitry can be a major issue. Since it would be challenging to evaluate the operation statuses of the optrode from external medical imaging instruments such as computed tomography (CT) scans, it becomes vital to incorporate a dedicated diagnostic sensing circuitry so as to be able to real-timely assess the optrode.

Therefore, in this thesis, a (µLED) sub-threshold voltage scan is proposed and performed at each stimulation site to evaluate the continued usable status of the optrode without activating light emissions. Based on the evaluation outcomes, clinical staff or patients could notice whether there is a device breakage or element malfunction, and they can also decide whether an alternate µLED should be used instead. During the normal operation, there is a diode-like behaviour of the current profile through the µLED. However, if there are some damages to the optrode, such as a mechanical fracture or contact corrosion between the µLED and CMOS circuits, the behaviour will differ significantly. These abnormalities can be detected by scanning current through each µLED and characterising their *I-V* profiles. For contact corrosion, it is expected that there would be massive µLED serial resistance, and thus the diode behaviour will be more linear. If a substrate fracture occurs, an open circuit will then be detected.

In order to identify these two abnormal conditions, a diagnostic sensing circuit is proposed, and its general block diagram is shown in Figure 4.35. In this circuitry, a DAC is chosen to set different input voltages. Then, a current scanning scheme could then be achieved via a Trans-Conductance Amplifier (TCA), where the sensing current I_{Dia} is then fed through the particular µLED, to sense its working status. The voltage profile across that µLED (V_{Dia}) could be consequently extracted. Finally, the output voltage V_{Dia} is transmitted to an ADC via an analogue MUX. As it is

undesired to switch on the µLED during the diagnostic sensing operation, V_{Dia} should be below the turn-on voltage, and I_{Dia} is expected to be limited to the µA level.

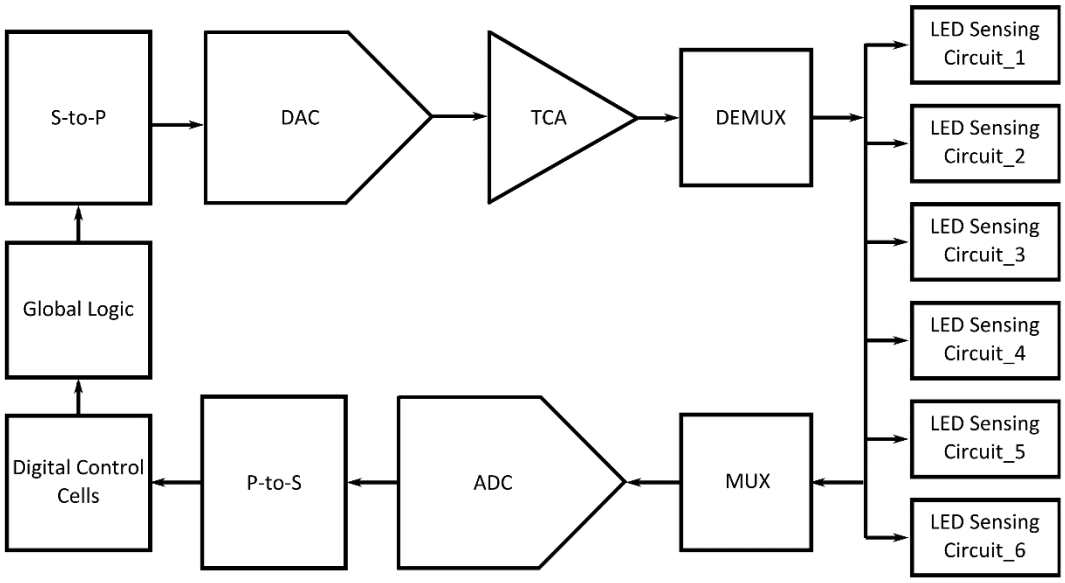


Figure 4.35 General block diagram of diagnostic sensing circuitry. The S-to-P interface is incorporated to receive external input voltages. These input voltages are then transmitted to a DAC module and converted to the weak sensing current I_{Dia} via the TCA. I_{Dia} is then fed through an analogue DEMUX to diagnose a particular µLED, LED_n. A diagnostic voltage V_{Dia} across that µLED could then be recorded and sent to an ADC via an analogue MUX. The recorded diagnostic voltage value would then be transmitted to external processors via a P-to-S interface.

In this thesis, some common circuit designs are used for both the stimulation circuitry and diagnostic circuitry, including µLED Driver, Pulse Width Modulator, DAC, and S-to-P interface, and these designs have been detailed in Section 4.2. This section describes and implements all of the main circuits which are only applied for the self-diagnosis function. All the dedicated modules required by the diagnostic sensing circuitry are listed below.

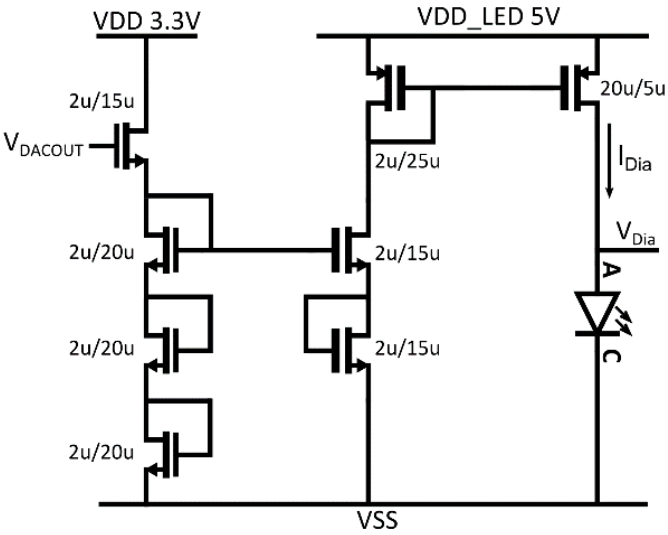
- Trans-Conductance Amplifier
- Analogue to Digital Converter
- Serial to Parallel Interface

This section is organised as follows: Subsection 4.3.2 describes a TCA design which could achieve the 'weak' sensing current I_{Dia}. Following that, the design and implementation of different types of ADCs are specified in Subsection 4.3.3. Subsection 4.3.4 then introduces the complementary P-to-S interface of the ADCs, and Subsection 4.3.5 summarises this section.

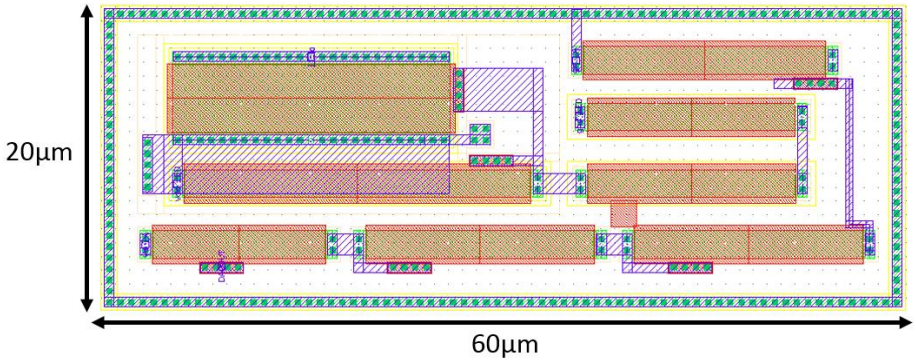
4.3.2 Trans-Conductance Amplifier

As depicted above, for diagnostic purposes, a ‘weak’ sensing current is demanded to flow through each stimulation site to generate a diagnostic voltage V_{Dia} across the specific µLED. By characterising µLED *I-V* profiles, any abnormal operation could consequently be detected. In order to extract these *I-V* profiles of the µLEDs, a voltage-driven current scanning approach is investigated, and a 3.3 V DAC module is included to provide voltage scanning. After that, the input voltage needs to be converted into a ‘weak’ diagnostic current. This current should be able to drive and sense the 5 V µLED driver in ‘dark’ mode. However, there is a gap for an intermediate element to link the 3.3 V DAC and the 5 V µLED driver together.

Therefore, an 8-transistor step-up TCA is proposed here to fulfil the requirement mentioned above. Its schematic diagram is displayed in Figure 4.36 (a). This TCA consists of two main blocks: a diode-connected voltage input stage, and a current output stage. The voltage input stage uses four 3.3 V N-MOSFETs, and the current output stage consists of four 5 V transistors. By employing this TCA, voltage shifting and current conversion functions are simultaneously realised.



(a)



(b)

Figure 4.36 The proposed 8-transistor 3.3 V to 5 V step-up TCA. (a) Schematic diagram. It mainly consists of two parts: the diode-connected 3.3 V voltage input stage, and the 5 V current output stage. A µLED model is included in this diagram. (b) Layout diagram. A guard ring is used to isolate the circuits from digital parts. The block dimensions are only 20 µm × 60 µm.

DC analysis is then executed to validate the functioning of this TCA, and the correlations between I_{Dia} and V_{DACOUT} are displayed in Figure 4.37. It can be observed that I_{Dia} varies quadratically from 0 µA to 11 µA while V_{DACOUT} is swept from 0 V to 3.3 V. It should be noted that V_{Dia} is strictly regulated below the µLED turn-on voltage by the given restrained I_{Dia}. Therefore, thanks to the tiny value of I_{Dia}, the µLED will maintain the 'dark' state constantly during diagnostic operations, and the sensing circuitry will perform in a highly safe region.

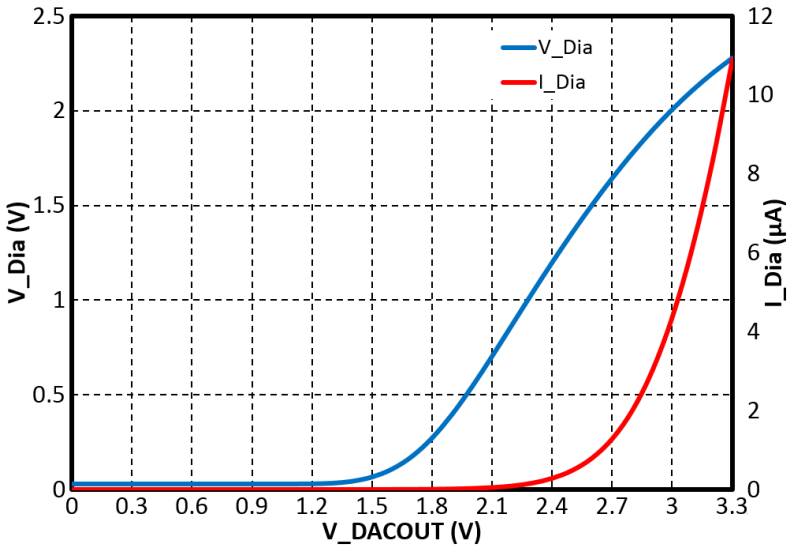


Figure 4.37 Correlations between I_{Dia}, V_{Dia} and V_{DACOUT}. The blue line represents the V_{Dia}, and the red line stands for the I_{Dia}. When V_{DACOUT} is gradually tuned from 0 V to 3.3 V, V_{Dia} increases from 0 V to 2.3 V, and I_{Dia} increases from 0 µA up to 11 µA.

Frequency analysis is conducted as well, as shown in Figure 4.38. And this step-up TCA achieves a 10.2 KHz 3 dB bandwidth, which is satisfactory for diagnostic operations.

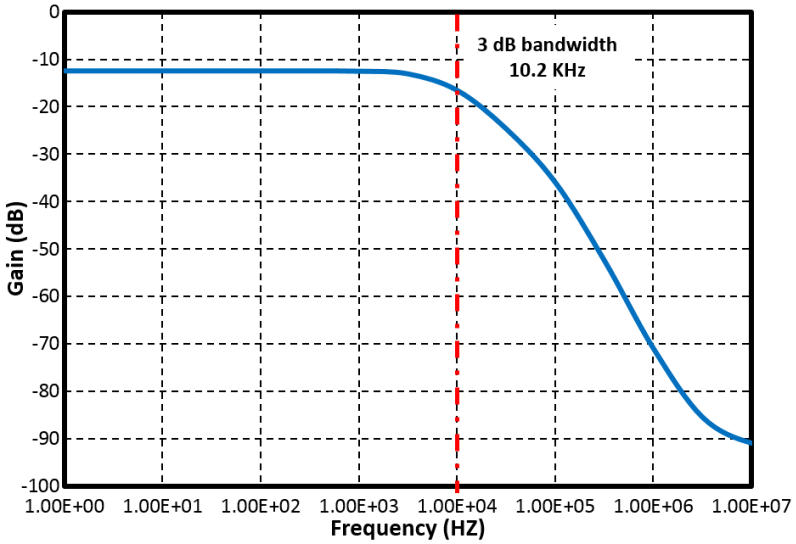


Figure 4.38 The frequency analysis of the TCA, obtained a 10.2 KHz 3 dB bandwidth.

Besides, power analysis is also performed to prove whether the power consumption of this TCA remains within a reasonable range. The calculated total power usage is 1.12 µW without diagnostic µLED power (12.7 µW on average). In particular, 0.26 µW is cost by the 3.3 V input circuitry, and 0.86 µW by the 5 V output circuitry. This indicates that this TCA has an ultra-low power costs. In the future, a feedback loop structure and power-gating strategy could be utilised for further optimisation.

Table 4.9 Main parameters of the TCA design for diagnostic circuitry.

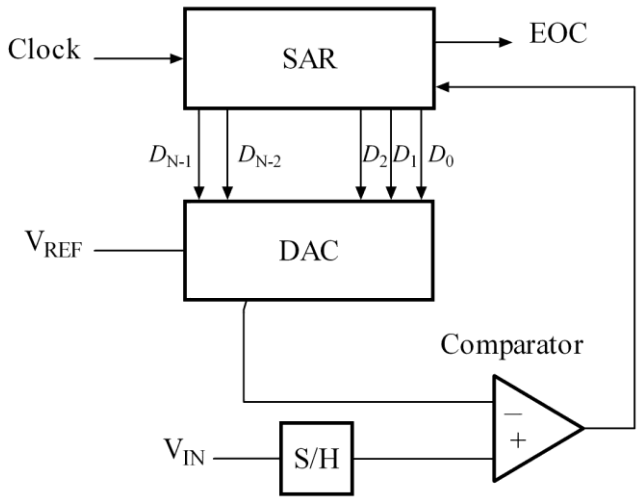
Technology	AMS 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V & 5 V
Circuit area	20 µm × 60 µm
Input voltage range	0 - 3.3 V
Output current range	0 - 11 µA
Maximum power consumption	1.12 µW

4.3.3 Analogue to Digital Converter

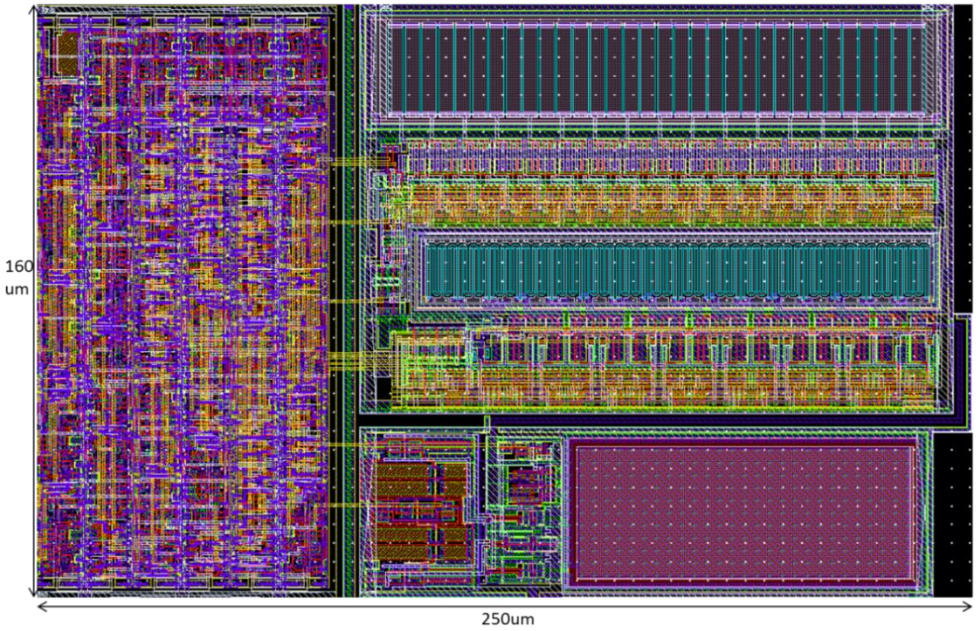
To accomplish the diagnostic circuitry, an ADC module is needed to fetch the diagnostic voltage V_{Dia}. Thus, this subsection presents two types of ADCs which can be used for optrode implementations. In Subsection 4.3.3.1, an off-the-shelf Successive Approximation Register (SAR) ADC is introduced and analysed. At the same time, in Subsection 4.3.3.2, a compact sigma-delta (ΣΔ or delta-sigma, ΔΣ) ADC is investigated and realised. Subsection 4.3.3.3 then summarises this subsection.

4.3.3.1 SAR ADC

The SAR ADC is widely utilised for medium to high-resolution applications. It can provide a relatively high sampling rate. By using a binary search algorithm, each possible quantization could be individually gone through until converged on the final digital output [127, 130]. A typical SAR architecture mainly consists of four main blocks, and a simplified block diagram is illustrated in Figure 4.39. The first block is the sample & hold circuitry, which receives the analogue input voltage $V_{IN.}$ After that, an N-bit DAC is employed to generate a series of analogue signals from the SAR logic block. The DAC output is then compared with the output of the sample & hold circuitry. An analogue voltage comparator is used to accomplish the comparison. Subsequently, the comparison result is fed back into the SAR logic block for data readjustment until the DAC output converges to V_{IN}.



(a)



(b)

Figure 4.39 An 8-bit SAR ADC, adopted from the AMS 0.35µm C35B4 process, A_CELLS analogue library [131]. The DAC applied in this SAR ADC is the resistor string DAC presented in Subsection 4.2.6.1. (a) Simplified schematic. EOC stands for the end of conversion, S/H is short for sample & hold circuit, and V_{REF} functions as the internal reference of DAC. (b) Layout diagram. The circuit dimensions are 160 µm × 250 µm.

Because of its finer resolution, high sampling rate and reasonable area cost, this off-the-shelf 8-bit SAR ADC has been chosen from the AMS library and has been implemented in Chapter 5, Subsection 5.3.4. The functionality of this SAR ADC is then validated by post-layout simulation, and the simulation results are shown in Figure 4.40, with the main specifications summarised in Table 4.10.

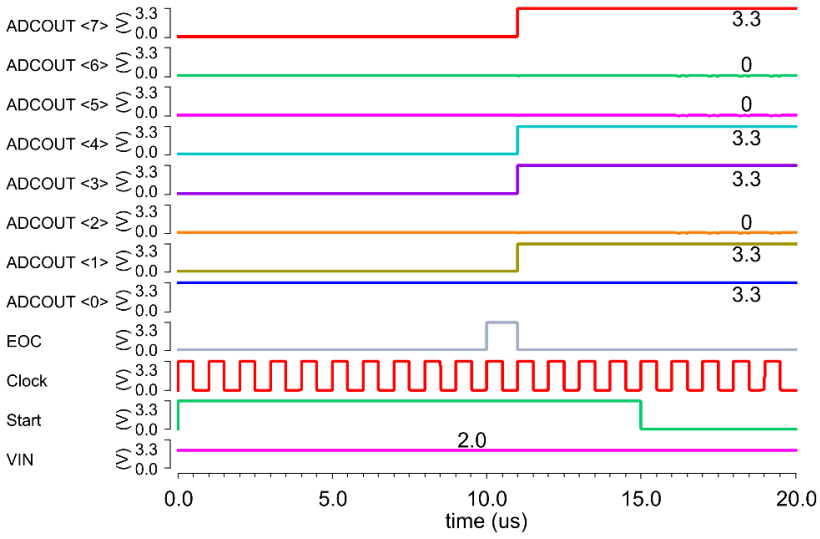


Figure 4.40 Post-layout simulation results of the AMS 8-bit SAR ADC. A random input V_{IN} is chosen as 2.0 V to verify the performance, and the corresponding digital output is <10011011>.

Table 4.10 General parameters of the AMS 8-bit SAR ADC.

Technology	AMS 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V
Resolution	8 bit
Input voltage range	0 - 3.3 V
Input impedance	(min) 100 MΩ
Different nonlinearity	±0.25 LSB
Integral nonlinearity	±0.25 LSB
Positive reference voltage	3.3 V
Negative reference voltage	0 V
Circuit area	160 µm×250 µm
Static power consumption	348 µW
Dynamic power consumption	1.2 mW (@ 1 MHZ)
Conversion time	9 µs
Clock frequency	(max) 1 MHZ
Settling time of S & H	(max) 1 µs

It can be noted that this SAR ADC has an appropriate resolution, and a suitable different & integral nonlinearity. It also possesses a compact ready-made layout, which largely saves on development time and resource costs. However, the total power consumption of this SAR ADC is an inevitable limitation for low energy implantable operations. Although this ADC is an acceptable choice for a proof-of-concept optrode design, it is not feasible for clinical applications hereafter. Thus, different low-power ADC development approaches need to be studied and implemented in future designs.

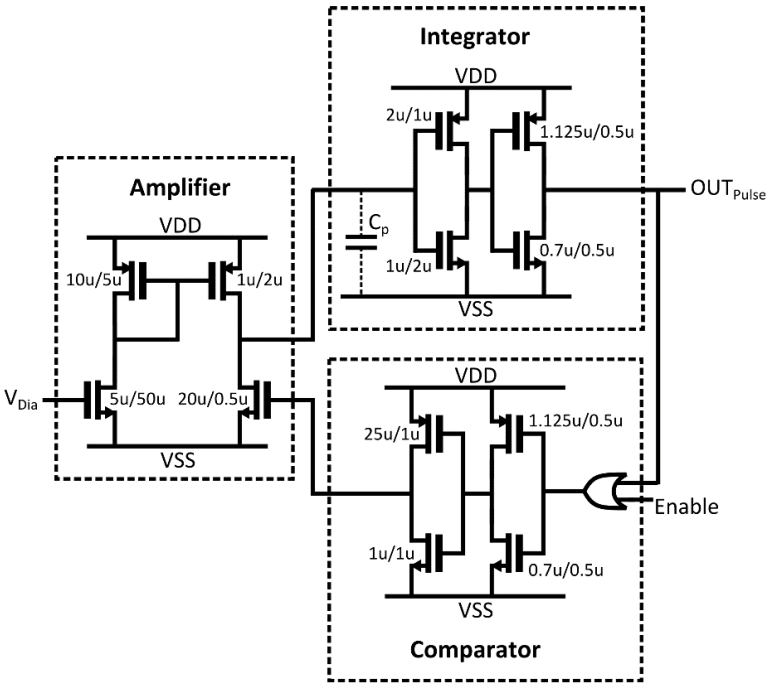
4.3.3.2 Sigma-Delta ADC

The previous subsection has presented a typical SAR ADC. It can be noted that the total power consumption of this particular ADC becomes problematic, especially for long-term implantable clinical applications. Also as those ADC outputs are formed in parallel, there is a need for a P-to-S converter (implemented in Subsection 4.3.4) to transform the output data into serial modality. This results in further energy

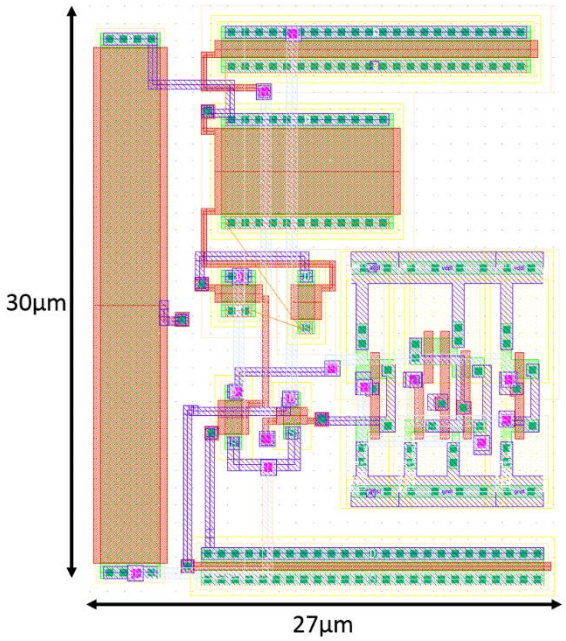
and area expenses. Additionally, even though the dimensions of this SAR ADC are reasonable, it is desirable to be miniaturised further.

Therefore, in this part, a distinct methodology, sigma-delta (ΣΔ, or delta-sigma ΔΣ) modulation, is considered to develop a low-power miniature ADC. ΣΔ modulation is a specific method used to encode analogue signals into digital signals, and it has been widely applied into ADC designs [132, 133]. The ΣΔ ADC converts an analogue voltage into a pulse/frequency modality, and counts the out pulses with a predefined time interval. This interval can be configured with a particular resolution. Then the pulse count, which is divided by the fixed interval, gives a precise digital output expression of the analogue input voltage [132, 133].

Here, the ΣΔ modulation technique is adapted into a one-port ADC design, and the circuit schematic is shown in Figure 4.41. This ΣΔ ADC primarily consists of three modules. The first module is a 4-transistor amplifier which can buffer and amplify the analogue input voltage V_{Dia}. Then the transformed input is transmitted to an integrator block. This integrator is mainly based on an inverter chain and a parasitic capacitor C_p. Once the integrated value reaches the threshold of the integrator, an out pulse is then triggered at the output port. At the same time, it is also directed into the comparator block. Consequently, the comparator resets the integrated value to zero, and the integration process is then repeated. Thus, the digital output pulse could be generated continuously. If the input voltage is higher, then the integration time will be accordingly shorter; otherwise, it will be longer. Therefore, the time interval between each two output pulses will relate to the input voltage V_{Dia}. Through this scheme, the analogue voltage could be correspondingly recorded via digital pulse expressions.



(a)



(b)

Figure 4.41 Proposed 1-port ΣΔ ADC. (a) Circuit schematic. This design only uses eighteen transistors, including the OR gate. (b) Layout diagram. The circuit dimensions are only 30 µm × 27 µm.

Then, a post-layout simulation is performed to certify its functionality, and the simulation results are illustrated in Figure 4.42. By tracing this simulation, the correlation between the input voltage and time interval ($t_{interval}$) could be deduced

subsequently, and the relationship is demonstrated in Figure 4.43. It can be seen that $t_{interval}$ has a large dynamic range from 10 ns to more than 10^6 ns (> 100 dB).

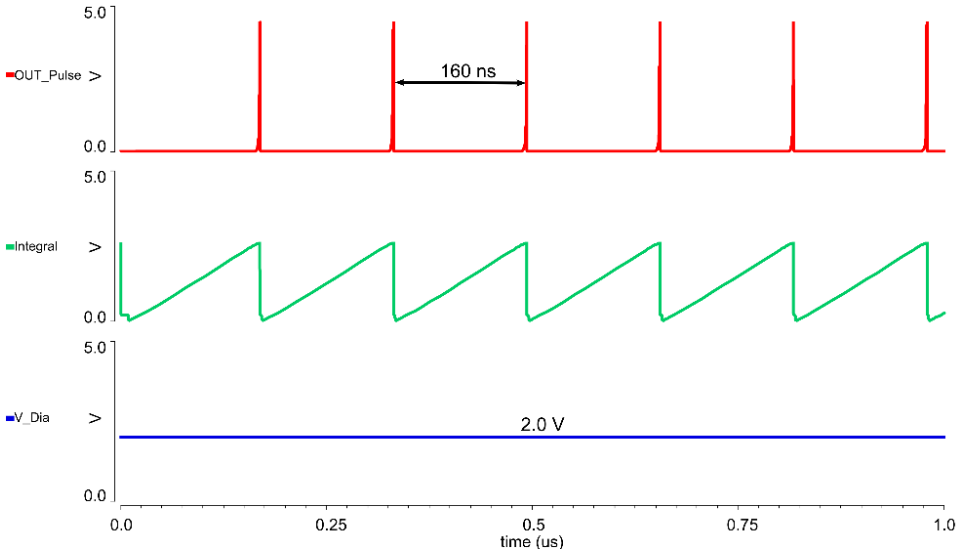


Figure 4.42 Post-layout simulation results of the proposed 1-port ΣΔ ADC. A random analogue input voltage is set to 2.0 V, and then a 160 ns time interval between each two output pulses is recorded.

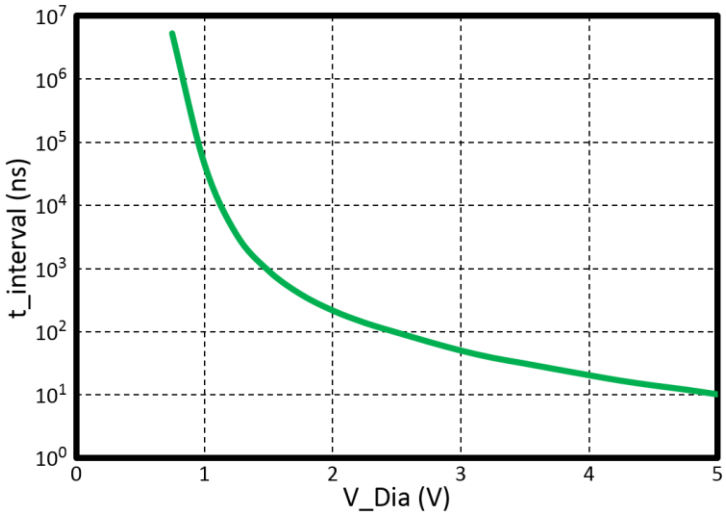


Figure 4.43 Relationship between time intervals of the output pulse versus the analogue input voltage. The $t_{interval}$ has a large dynamic range from nanoseconds to milliseconds, which provides an outstanding sampling resolution.

Power analysis is also performed, and the average power consumption has been calculated. When this ADC operates with a 5 V power supply, the power consumption is 12.6 µW. When supply voltage decreases to 3.3 V, the power cost is then reduced to 4.8 µW. Thus, this ΣΔ ADC demonstrates an appropriate power dissipation performance. Similar to the pulse modulated DAC, in actual use, the

maximum operation frequency of this ΣΔ ADC is determined by the external controller (FPGA), i.e. 100 MHz in this work.

To conclude, this one-port ΣΔ ADC has a simple and compact structure, small dimensions, large dynamic range, efficient energy consumption, and it can correctly extract the analogue diagnostic voltage via pulse modalities. Because of these strengths, this ΣΔ ADC has been implemented in Chapter 5, Subsection 5.2.4.

Table 4.11 Main parameters of the ΣΔ ADC.

Technology	X-FAB 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V/5 V
Input voltage range	0 - 3.3 V/0 - 5 V
Output pulse resolution	10 ns
Dynamic range	> 100 dB
Circuit area	30 µm×27 µm
Static power consumption	1.6 fW/3.3 fW
Dynamic power consumption	4.8 µW/12.6 µW
Clock frequency (FPGA)	(max) 100 MHz

4.3.3.3 Summary

In this subsection, a SAR ADC and a ΣΔ ADC are separately investigated. The performance comparison between these two ADC designs is summarised in Table 4.12. Nowadays, the SAR type of ADC has been widely utilised, owing to its moderate design complicacy, fast conversion speed, finer resolution, reasonable area, and power requirement. However, for the particular SAR ADC introduced in Subsection 4.3.3.1, because of the utilisation of the resistor string DAC, the overall power consumption becomes problematic. In the future, new SAR ADC topologies, therefore, will need to be investigated, such as a charge-redistribution SAR ADC, in order to reduce the energy budget. Moreover, a ΣΔ ADC has also been explored. This one-port ΣΔ ADC has a compact structure using only eighteen transistors, and its power consumption is suitable for both 3.3 V and 5 V circuitry. Also, it avoids the need for a P-to-S interface. More importantly, it has a wide dynamic range of pulse intervals, which guarantees precise data recording. But there are still some recommendations for future improvements. In the future, a downstream counter can

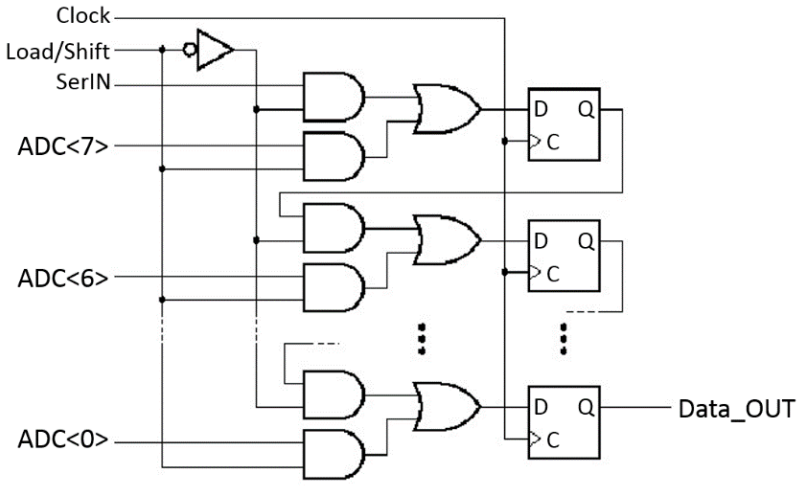
be incorporated to decode the output into a more convenient format. And a dedicated decoding structure could be developed to interpret the location information of the ΣΔ ADC in each channel.

Table 4.12 Performance comparison of the two ADC designs.

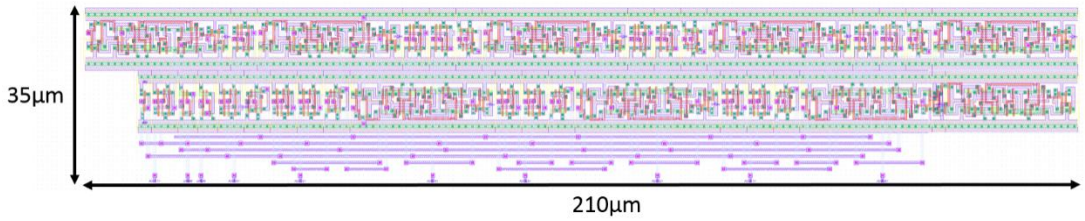
ADC	SAR ADC	ΣΔ ADC
Technology	AMS 0.35-µm, 2P4M CMOS	X-FAB 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V	3.3 V/5 V
Input voltage range	0 - 3.3 V	0 - 3.3 V/0 - 5 V
Dynamic range	48 dB	> 100 dB
Circuit area	160 µm×250 µm	30 µm×27 µm
Static power consumption	348 µW	1.6 fW/3.3 fW
Dynamic power consumption	1.2 mW	4.8 µW/12.6 µW
Clock frequency	(max) 1 MHz	(max) 100 MHz

4.3.4 Parallel to Serial Interface

In this subsection, an 8-bit P-to-S interface is implemented for the 8-bit SAR ADC. Figure 4.44 (a) shows a simplified schematic diagram of the parallel-in, serial-out converter. It primarily contains a series of D flip-flops, combined with some supplementary logic elements which are mainly AND gates and OR gates to construct a 2-input multiplexer chain. Depending on the value of Load/Shift, the D flip-flop will be configured (via the 2-input multiplexer) to either receive the new data from input ports or to shift its current value to the next bit.



(a)



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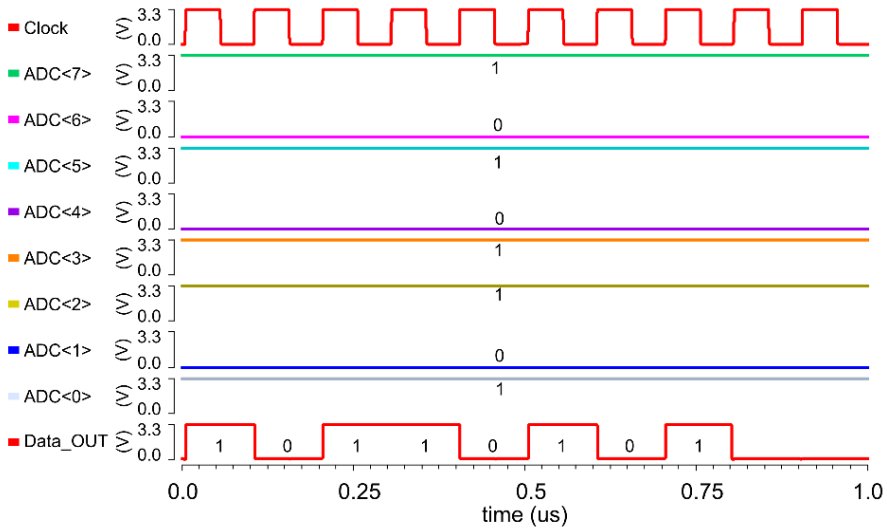


(c)

Figure 4.44 (a) Simplified design diagram of the P-to-S interface. (b) Layout of the P-to-S converter, including accessory logic cells. The circuit dimensions are only 35 µm × 210 µm. (c) Simulation results of the P-to-S conversion. A random input data string is chosen as {10101101}, and after eight clock cycles the conversion is then finished.

4.3.5 Summary

This section has focused on the development of the dedicated circuits for the diagnostic sensing function. A general architecture of the diagnostic sensing circuitry has been demonstrated at the start. Then individual components have been detailed in subsequent subsections. An 8-transistor step-up TCA has been built to illustrate the µLED *I* - *V* profile in the 'dark' region, and this TCA is compatible with both 3.3 V and 5 V power sources. By extracting the voltage profile across the µLED anode, the real-time operational status of each stimulation site could be noticed. Therefore, two types of ADC have been explored and developed to record the diagnostic voltages. Limitations of both ADC designs have been pointed out, and recommended future work has also been highlighted. Additionally, a supplementary P-to-S interface has been created to complete the system design. All of the circuits described in this section have been applied for the constructions of diagnostic sensing circuitry within different optrodes in Chapter 5.

4.4 Conclusion

This chapter has detailed both the optical stimulation circuitry and diagnostic sensing circuitry at component level. Different circuit designs have been created and are listed below.

- µLED Driver (Stimulation & Diagnostic)
- Pulse Width Modulator (Stimulation & Diagnostic)
- Inverting Voltage Amplifier (Stimulation only)
- Digital to Analogue Converter (Stimulation & Diagnostic)
- Serial to Parallel Interface (Stimulation & Diagnostic)
- Level Shifter (Stimulation only)
- Trans-Conductance Amplifier (Diagnostic only)
- Analogue-to-Digital Converter (Diagnostic only)
- Parallel to Serial Interface (Diagnostic only)

Single-direction and bi-direction µLED drive circuits have both been investigated, to meet the requirements of the targeted light delivery. In particular, the H-Bridge topology has been adapted for biphasic optical stimulation and diagnostic sensing. It would also be utilised for future investigations of the electrical characteristics of the µLED, when it is in the reverse-biased condition. In order to programme the light intensity, the PWM method has been employed. Three types of pulse width modulators have been explored and utilised to regulate the light intensity of the emitters. These pulse width modulators also been act as memory units to configure the operational states of the stimulation and diagnostic circuitry. Apart from the PWM scheme, the intensity magnitude modulation strategy has also been introduced to further improve light intensity controllability and optical emission efficiency. Different DAC topologies have been studied and realised for intensity magnitude modulation. These DAC elements have also been adopted for the self-diagnosis function, achieving *I* - *V* sweeping across each stimulation site so that the real-time µLED working behaviours can then be observed. Relevant limitations of each DAC design have been identified, and potential optimisation solutions have also been suggested. In the meantime, a dedicated 5-transistor step-up Inverting Voltage Amplifier has been created to link the 3.3 V DAC with the 5 V µLED driver. Similarly, an 8-transistor step-up TCA has been developed for the diagnostic sensing

side, converting the 0 - 3.3 V DAC input voltage into a 0 - 11 µA ‘weak’ diagnostic sensing current. Then, during system self-diagnosis, the *I* - *V* profile of µLED would be built in ‘dark’ mode, and the diagnostic voltage could be consequently extracted. In order to record the diagnostic sensing voltage, ADC modules have been formed. Two different ADC design strategies have been employed, and both designs have been implemented into different optrodes. Their weaknesses have also been observed, and related enhancing work could be conducted in the future. In addition, peripheral elements, such as S-to-P, P-to-S, and level shifter, have been generated to perfect the system.

All these circuits mentioned above have been thoroughly analysed and developed, with simple structures, compact layouts, reasonable power consumptions, and the expected functionalities. This chapter provides an abundant component library for the proposed optogenetic implants. Chapter 5 next elaborates the construction of different versions of optrodes, using all the circuits presented here. It also shows how to combine these existing circuits with external functioning circuits to realise an advanced multi-functional implantable optrode.

Chapter-4 Contributions

Contributor	Contributions
Mr Hubin Zhao	1) Defined all the circuit components of the optrode 2) Designed, implemented, and verified all the circuits of the optical stimulation circuitry* 3) Designed, implemented, and verified all the circuits of the diagnostic sensing circuitry* * Except the AMS resistor string DAC and SAR ADC

5 System Implementation

5.1 Introduction

The previous chapter detailed the design and implementation of each component utilised in optrode developments in this study. The proposed optrode aims to achieve precise light delivery and multi-site optical stimulation. Moreover, it is vital to include a sophisticated sensing circuitry which could assess the system mechanical integrity and detect any malfunction of light emitters. Furthermore, for this CMOS-driven μLED-on-optrode approach, the thermal effects associated with μLEDs need to be considered, as this is critical for both circuitry stability and patient health. Besides, it is desirable and important to integrate external neural recording circuitry into the optrode. This neural recording circuitry could provide simultaneous feedback neural signals for the optical stimulator. And an advanced optical-electro closed-loop neural interface should be accomplished.

To meet the design criteria depicted above, diverse functioning circuitries are required to be integrated into the proposed optrode, including optical stimulation circuitry, diagnostic sensing circuitry, thermal sensing circuitry, and neural recording circuitry. Thus, the focus of this chapter is to elaborate on the implementation of each functioning circuitry and to perform corresponding system integrations, and then to complete the implementation of the proposed multi-functional optrode.

This chapter is organised as follows: Section 5.2 presents the first version of the CMOS-driven μLED optogenetic implant. It realises local optical stimulation in multi-site regions, and the light intensity can be adjusted via the PWM method. In particular, for the first time, the self-diagnosis strategy is created to monitor the operational status of the implant. This provides a significant enhancement of the system safety and stability. In Section 5.3, based on the first version, an updated CMOS optrode is developed. The bidirectional μLED driver is first time adopted for optical stimulation. The direct current/intensity control strategy is incorporated along with the updated PWM structure, obtaining finer overall light intensity modulation. Furthermore, the self-diagnostic circuitry is correspondingly modified to achieve higher-resolution and lower-current operation. Moreover, a resistive temperature

sensor is also included into the updated optrode which can evaluate the thermal effect of light emitters, ensuring both system reliability and patient safety. Besides, external electrical neural recording circuitry is combined with the optical stimulator to realise a feedback-loop neural processing platform. Section 5.4 then briefs the external support required for optrode post-processing. Section 5.5 concludes this chapter.

5.2 Open-Loop Optrode for Optical Neural Stimulation

This section presents an open-loop CMOS active optrode for optical neural stimulation. This design is the first prototype of the CMOS-based active optogenetic implant. It proves the feasibility of the CMOS-driven active optrode approach.

A conceptual diagram in Figure 5.1 demonstrates how this optrode can work with a standard chest pacemaker. This optrode mainly consists of three subsystems, including a communication & logic control subsystem, a stimulation control subsystem and a diagnostic sensing subsystem. In the communication & logic control subsystem, an adapted SPI protocol is utilised for global addressing and logic control. The stimulation control subsystem, as elaborated later, primarily contains separately addressable μLED drivers with individual memory units, which could generate a high current for multi-site stimulation and accomplish the PWM of light intensity. To achieve the self-diagnostic function, a sub-threshold voltage scanning is performed across the μLED. This diagnostic function could detect system operational degradations. In particular, it could identify the optrode rupture situation, without triggering light emission, and any failure of light emitters could also be discovered. Consequently, the patient or support technician could decide whether to switch off the faulty stimulation site and to turn on an alternate channel. Thus, this diagnostic sensing strategy could profoundly improve the operational stability and safety of the optrode.

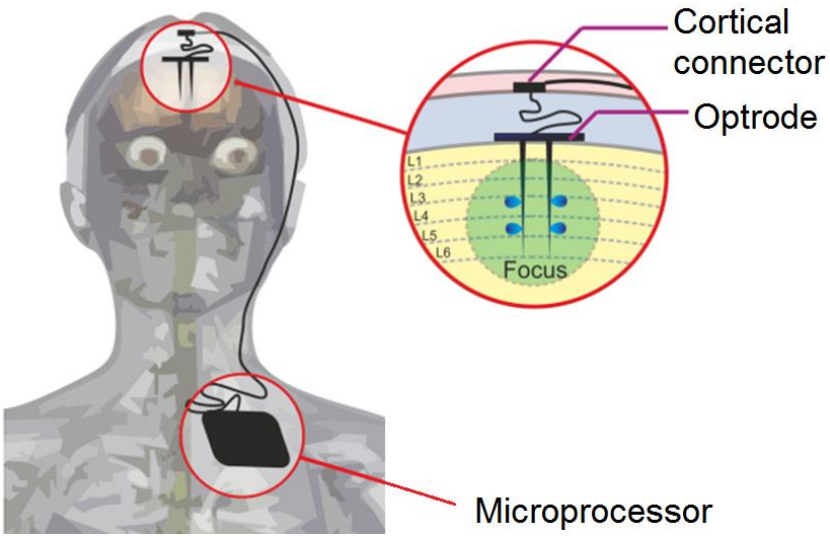


Figure 5.1 Conceptual diagram of the implantable optrode. This proposed CMOS optrode could achieve multi-site and multi-layer stimulation. It would be controlled by a chest biomedical microprocessor via a cortical connector.

5.2.1 System Architecture

This subsection describes the global architecture of this proposed open-loop optical neural probe, and the floorplan diagram is shown in Figure 5.2. It can be seen that this optrode mainly consists of two parts: the optrode head in which all of the active circuits are included, and the CMOS/silicon-based optrode shaft. The dimensions of the optrode shaft are defined as 4.4 mm × 200 μm, to match the thickness of brain cortical layers. This also guarantees the sharpness of the optrode shaft, which could potentially diminish tissue damage during implantation.

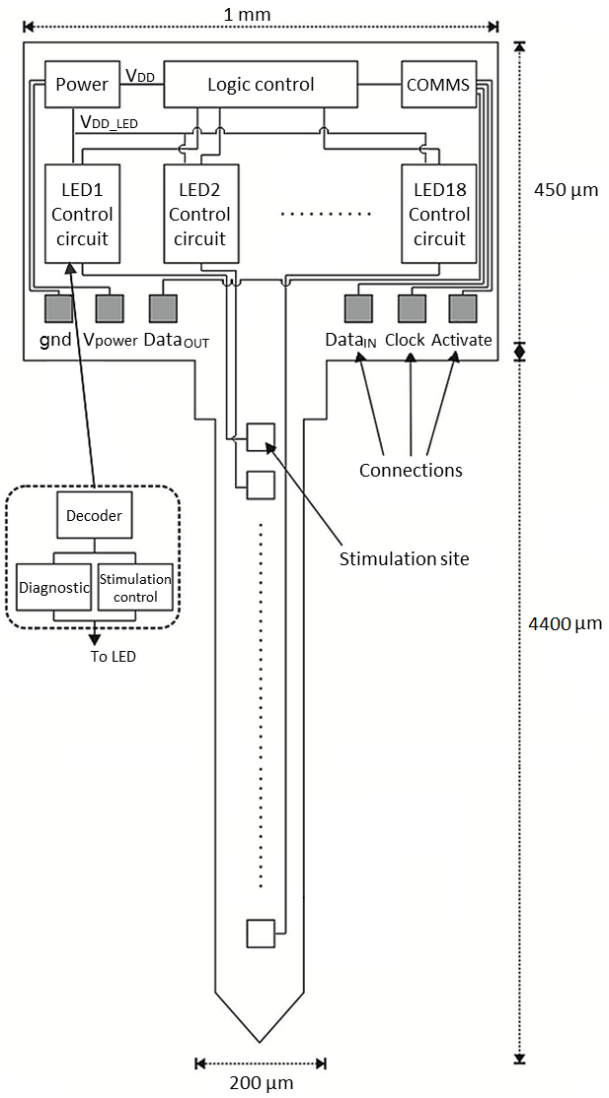


Figure 5.2 System architecture of the open-loop optical probe. All the CMOS circuitry is fitted into to the 450 µm × 1000 µm optrode head area, which ensures the miniature size of the probe. The width of the optrode shaft is set as 200 µm. This ensures tip sharpness, which would be beneficial for reducing tissue damage caused by physical implantation.

In order to achieve multi-site/multi-layer optical stimulation, six stimulation sites have been evenly positioned on the optrode shaft. Three µLEDs are placed in each stimulation site to construct a µLED cluster. In each cluster, the middle µLED functions as the main µLED, while other two auxiliary µLEDs act as backups. By employing this backup mechanism, the longevity and robustness of each stimulation site can be enhanced, and the µLED light intensity and stimulation penetration area would become more tuneable. In the head part, eighteen µLED control modules are generated to access and operate the individual eighteen µLEDs. Each µLED control module can perform both stimulation control function and diagnostic sensing function. Moreover, in order to address and control the whole system, a global

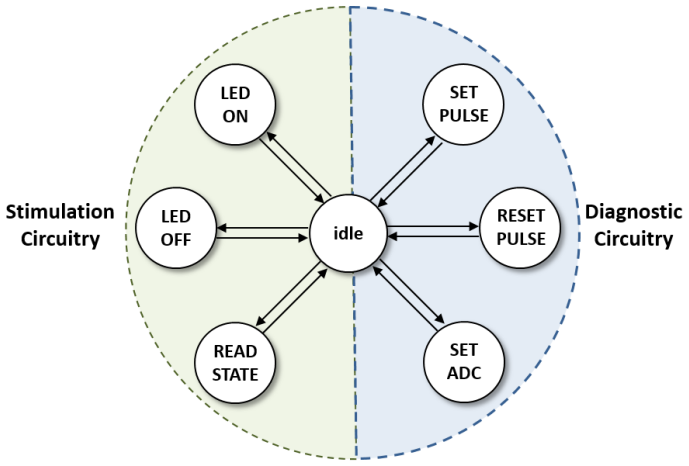
communication and logic control module is implemented in the head part. This determines all of the input/output data of the optical stimulation circuitry and the diagnostic sensing circuitry. Subsequently, each μLED point could be individually controlled and sensed. In addition, six I/O pads are implemented to either convey input/output signals or provide power supplies.

5.2.2 Logic Control

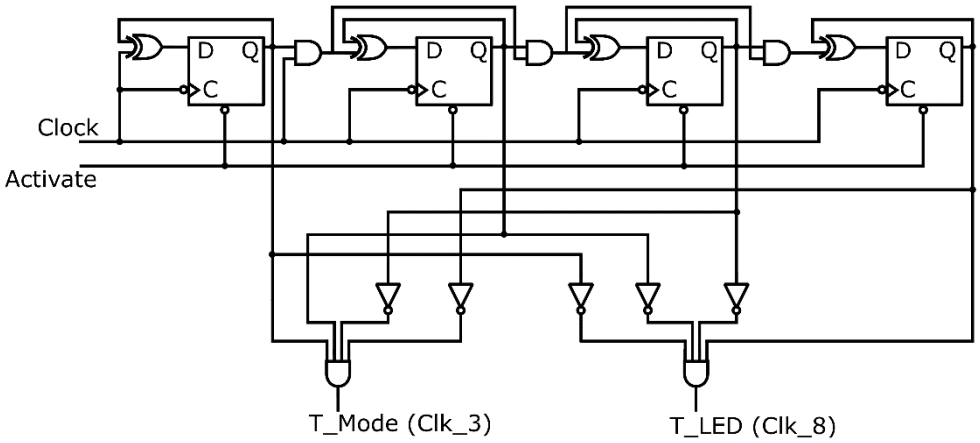
In the logic control subsystem, an SPI protocol has been tailored and utilised for two-way communication and data transmission. By using a standard communication protocol, the optrode can be easily accessed and controlled by either a FPGA or microcontroller unit. In this adapted SPI bus, a global clock signal is defined to synchronise all the logical operations of the optrode. And an external activate signal determines the state of a particular operation, which will be either asserted or negated. Related input and output data paths are designed to convey both internal and external information bilaterally.

Figure 5.3 displays a schematic diagram of the logic control subsystem. Shift register, decoder and latch structure are applied to construct three primary functioning modules: Counter, Mode Selection and μLED Selection. All these modules are regulated by three external signals: *Activate*, *Clock* and $Data_{IN}$. The global *Clock* signal defines the system timing and operation frequency. The *Activate* acts as a primary enable signal, and it determines the state of each specific operation. The $Data_{IN}$ signal is utilised for serial data transmission. The Counter module mainly contains a series of falling edge D flip-flops, and it creates the *T_Mode* and *T_LED* signals to control the other two modules. In the Mode Selection module, six operation modes are then determined when *T_Mode* is enabled. LED_{ON} and LED_{OFF} are two major working patterns for the stimulation circuitry, and these two modes could manipulate the μLEDs with a predefined pulse width. The *Read* function is used to monitor the real-time status of the μLED via the pulse width modulator. *Set_Pulse* and *Reset_Pulse* are two input signals for the pulse modulated DAC (see Chapter 4, Subsection 4.2.6.2), which could achieve the voltage scanning scheme for diagnostic purposes. The *Set_ADC* is a trigger signal to enable or disable the ΣΔ ADC (see Chapter 4, Subsection 4.3.3.2). The ΣΔ ADC could then record the diagnostic sensing voltage, and the recorded data is then fetched via pulse

expressions. Once the operation mode is decided, the targeted μLED needs to be defined. Then, in the μLED Selection module, the active μLED, LED_n, is selected by decoding the address information from $Data_{IN}$, while the *T_Mode* is negated and *T_LED* is asserted.



(a)



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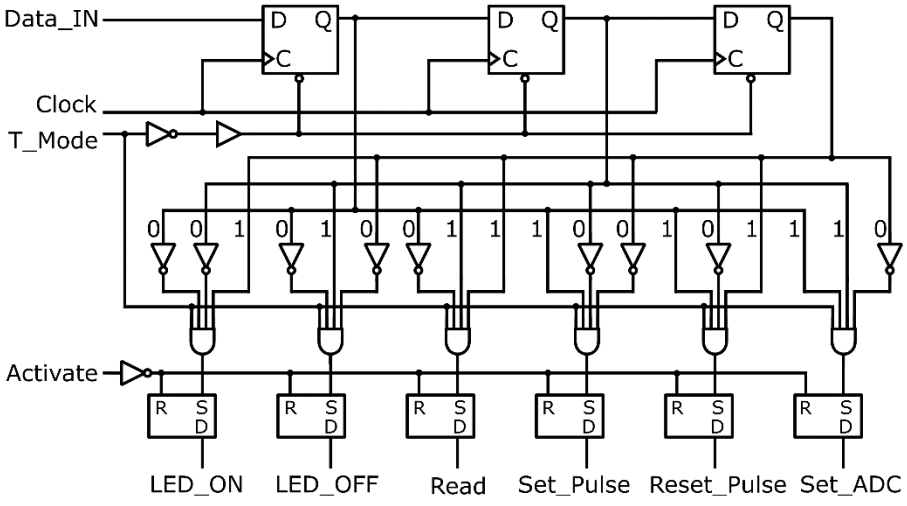

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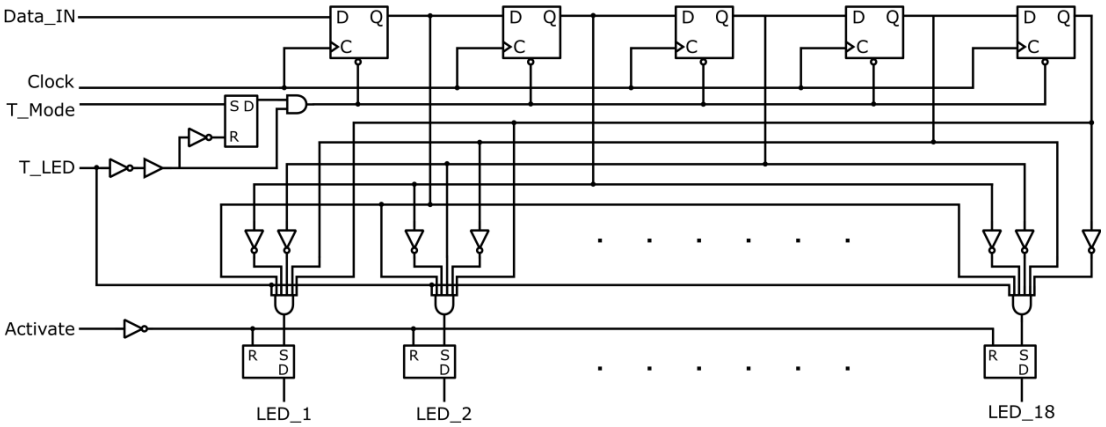


(d)

Figure 5.3 Schematic diagram of the logic control circuitry. (a) The logic command tree, which demonstrates the different optrode operation modes. (b) Counter module. It consists of two input signals, *Clock* and *Activate*, and it creates the *T_Mode* and *T_LED* for modes and µLED selections. (c) Mode Selection module. Six optrode operation modes are determined in this module. LED_{ON}, LED_{OFF}, and *Read* signals are responsible for the stimulation control subsystem, and *Set_Pulse*, *Reset_Pulse*, and *Set_ADC* signals determine the diagnostic sensing subsystem. (d) µLED Selection module. It includes eighteen µLED address indexes.

These three modules are constructed using standard digital cells. The layout diagrams are displayed in Figure 5.4. All of the layouts are manually completed to achieve a compact implementation. Their heights are configured as 35 µm uniformly. The total dimensions of the logic control subsystem are 35 µm × 570 µm, and so it can be easily fitted into the optrode head.

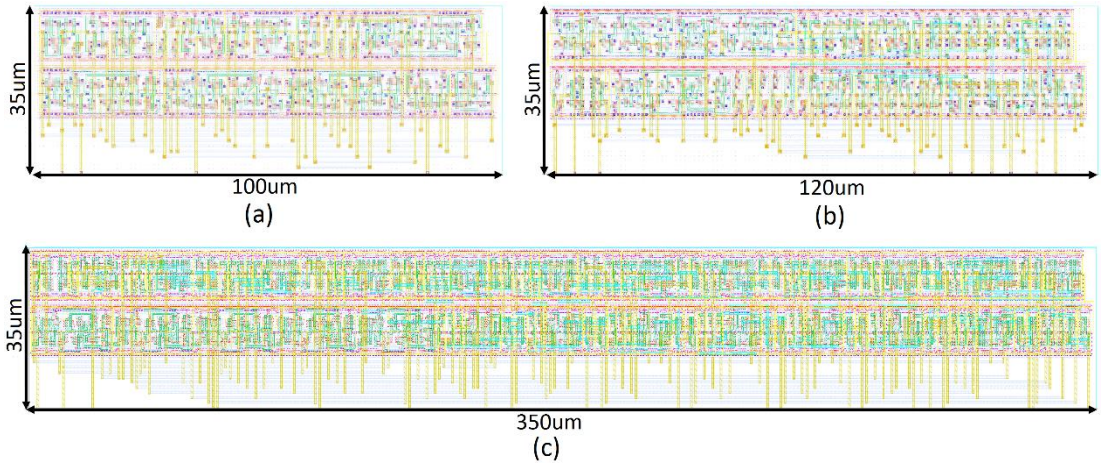
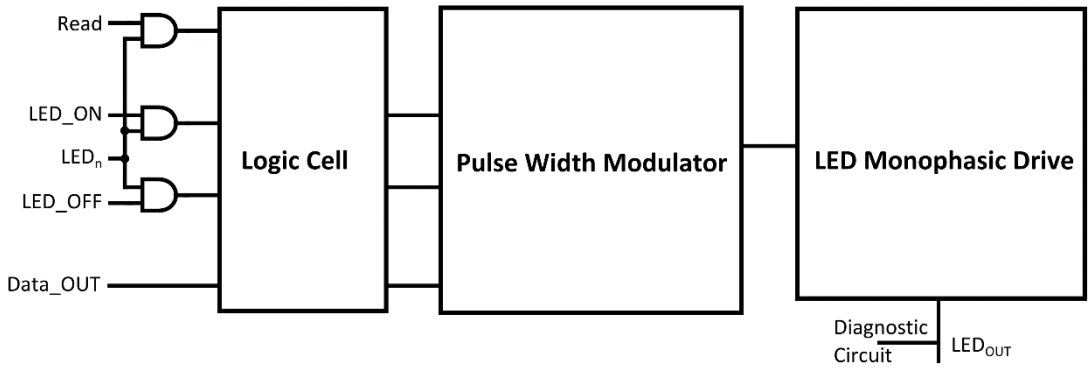


Figure 5.4 Layout diagrams of logic control modules. (a) Counter. The layout dimensions are 35 µm × 100 µm. (b) Mode Selection. The circuit area is 35 µm × 120 µm. (c) µLED Selection, with a 35 µm × 350 µm layout.

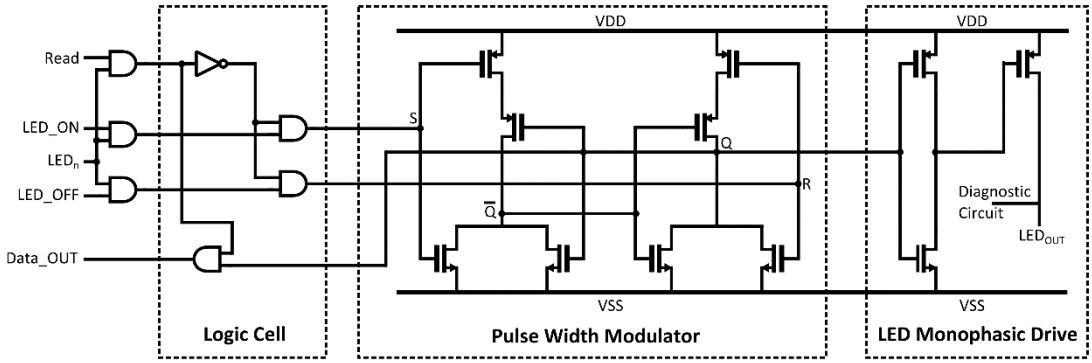
5.2.3 Stimulation Control Subsystem

The previous subsection has detailed the logic control subsystem, and in this part the focus moves to the implementation of the optical stimulation control subsystem. In this subsystem, eighteen stimulation control blocks are included to manipulate each µLED emitter locally. Through this configuration, local light delivery and multi-site stimulation become possible.

Each local stimulation control block mainly contains three modules: logic elements, pulse width modulator and µLED drive circuit. A schematic diagram of the local stimulation control block is shown in Figure 5.5. It can be observed that the stimulation operation is manipulated via the LED_{ON}, LED_{OFF} and *Read* signals along with the active µLED address index LED_n. The local logic element receives external signals and decodes them into the corresponding working mode index (LED_{ON} or LED_{OFF} or *Read*). Then the activated mode index is conveyed into the pulse width modulator. Consequently, the pulse width modulator saves the predefined operation state (either LED_{ON} or LED_{OFF}) and transmits it to the µLED drive circuit. The pulse width modulator retains this operation state consistently to maintain the stimulation cycle until new data is pushed in and a new working mode is updated. The *Read* signal observes the µLED real-time working state (ON/OFF) from the pulse width modulator, and then sends it to the $Data_{OUT}$ port. A wide transistor is utilised in the µLED driver to generate a high current flow driven by the 5 V power supply V_{DD_LED}, and this creates sufficient light emission when the working mode is $LED_{ON.}$



(a)



(b)

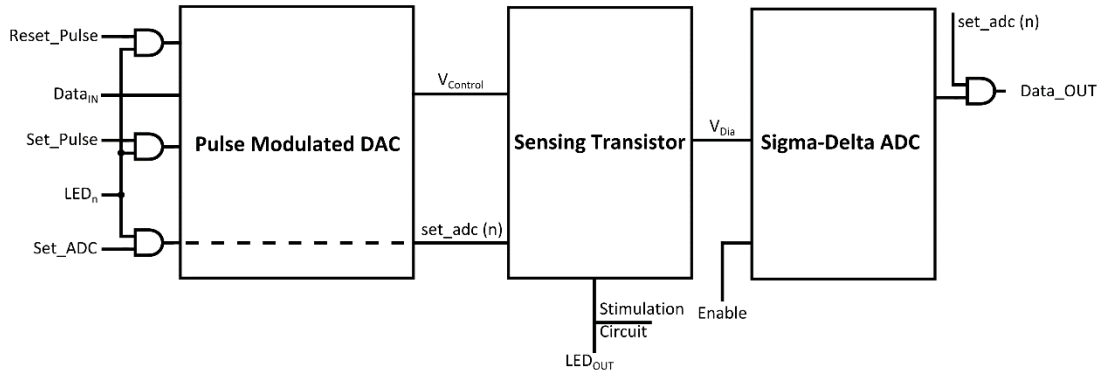
Figure 5.5 Schematic of local stimulation control circuitry. The logic cell decodes input signals and transmits the µLED operation state to the pulse width modulator. Based on the received state information, the pulse width modulator manipulates the µLED driver to control the particular light emitter. The *Read* signal monitors the real-time µLED working state saved by the pulse width modulator and sends the state information to $Data_{OUT}$. The pulse width modulator is adopted from Chapter 4, Subsection 4.2.4.1, and the µLED drive is chosen from Chapter 4, Subsection 4.2.2.2.

5.2.4 Diagnostic Sensing Subsystem

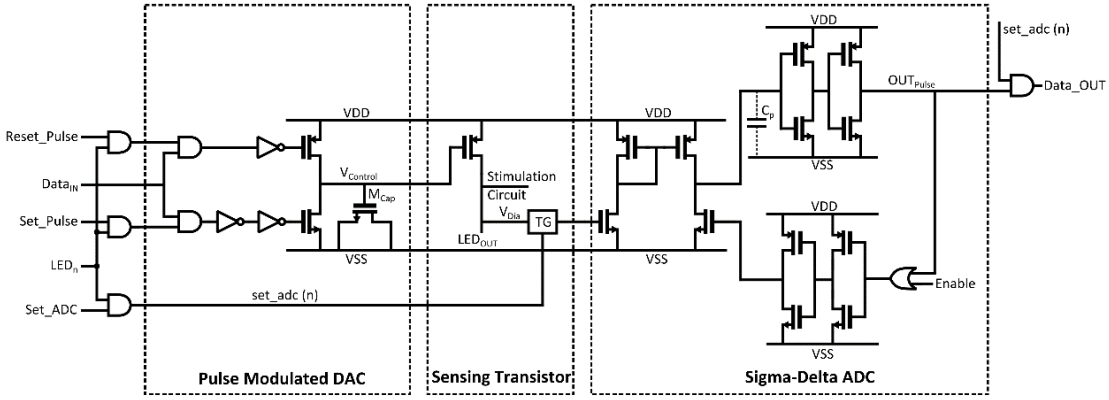
When the optrode is performing a standard light emission, the current feature of the µLED will behave like a diode. But if there is any malfunction, such as shaft rupture of the optrode or contact erosion between the light emitter and the CMOS circuitry, this can be revealed by the voltage profile generated at the stimulation point, which provides the basis of the self-diagnostic function. This function only can be performed when guaranteeing that the voltage at the stimulation site is lower than the µLED working threshold.

Hence, this subsection details the structure of the diagnostic sensing subsystem. This system also consists of eighteen diagnostic local sensing blocks, which guarantees that every light emitter could be independently accessed. In each diagnostic sensing block, three different functioning circuits have been realised. The first module is a pulse width modulated DAC (picked from Chapter 4, Subsection 4.2.6.2). This module determines the input of the sensing voltage, V_{Sense}. By tuning the input pulse, different values of V_{Sense} could be obtained. V_{Sense} is then applied on the second module of the local diagnostic block, a sensing transistor M_{diag}. M_{diag} functions as a current sensor at the stimulation site. Since this diagnosis function is expected to operate without activating light emission, M_{diag} is set at 10 µm/1 µm to limit the sensing current to a safe range. As this sensing current (I_{Dia})

has a quadratic relationship with V_{Sense}, it results in a large dynamic range when scanning the V_{Sense}. Subsequently, the diagnostic output voltage V_{Dia} is produced across the µLED anode, and this output voltage is read by the third module, a ΣΔ ADC (chosen from Chapter 4, Subsection 4.3.3.2). This ΣΔ ADC receives the diagnostic output V_{Dia} via an amplifier, and then converts this amplified output voltage into digital pulses. As explained before, the V_{Dia} has an inverse relationship with the time interval ($t_{interval}$), and thus the V_{Dia} could be noted and reconstructed by recording the $t_{interval}$.



(a)



(b)

Figure 5.6 Schematic diagram of the local diagnostic sensing block. *Set_Pulse* & *Reset_Pulse* signals define the input data for the pulse width modulated DAC to accomplish the voltage scanning operation. *Set_ADC* acts as an enable signal for the ADC block, and it performs the timing control of the ADC module.

A voltage-current scanning can thus be realised, and then the feature profile of the diagnostic voltage is generated at the particular stimulation site. If the resistance at that point increases, for example in cases of a contact erosion between the CMOS and the µLED, then the voltage feature curve will be more resistive. This larger resistance will make the V_{Dia} greater than the standard value, and it will result in a

considerably shorter $t_{interval}$ than expected. When the optrode rupture happens, an open circuit will be created above that point, the V_{Dia} will then be approximately equal to V_{DD_LED}, and the $t_{interval}$ will reach the lower limit value, 10 ns.

One point which should be noted is that, in order not to activate light emissions, selected sampling values of V_{Sense} are defined to 4.25 V, 4.0 V, 3.75 V, and 3.5 V; in other words, $|V_{gs}|$ ($|V_{gs}|$ is the difference between V_{DD_LED} and V_{Sense}) = 0.75 V, 1.0 V, 1.25 V, 1.5 V. To achieve this, the pulse widths of the *Set_Pulse* signal are limited within 200 ns.

5.2.5 Local Block Integration

Subsection 5.2.3 and Subsection 5.2.4 have described the stimulation control subsystem and diagnostic sensing subsystem respectively. This subsection explains the integration of these two subsystems. Since every stimulation site is controlled by both a stimulation control block and diagnostic sensing block, it would be convenient to mingle these two blocks locally rather than globally. As the µLED drive voltage V_{LED} and µLED sensing voltage V_{Dia} are applied on the same µLED, it is necessary to combine these two functioning circuits whilst discerning them via the analogue MUX and DEMUX.

Integrated local circuitry can significantly save on total circuit area, and Figure 5.7 displays a compact layout of a combined stimulation and diagnostic block. This implementation requires an area of only 50 µm × 90 µm, including all standard digital cells and custom analogue elements. A guard ring is used to separate the analogue part from the digital part to diminish the substrate noise. Because of the compactness of this layout, it makes the eighteen integrated local stimulation and diagnostic blocks feasible to be fitted into the 1 mm-wide optrode head, which ensures the miniaturisation of this optrode design.

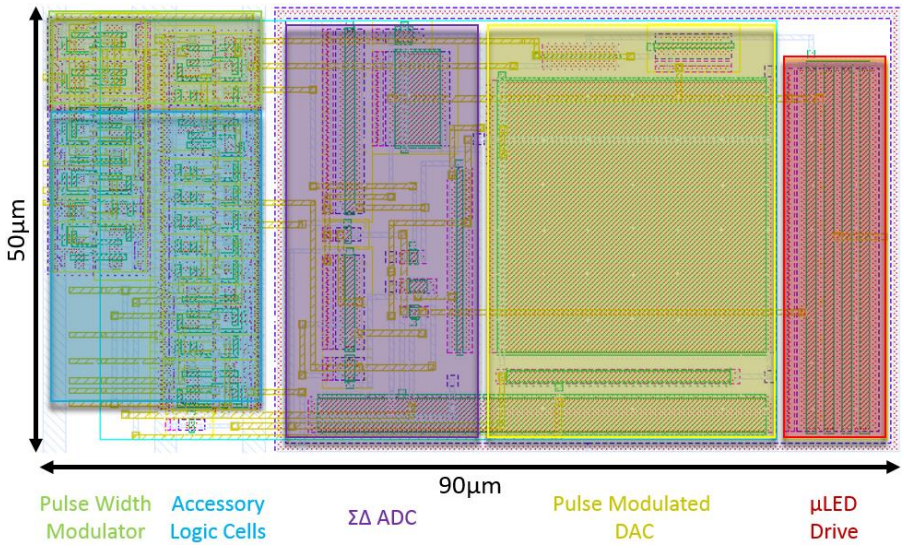


Figure 5.7 Layout of integrated local stimulation and diagnostic circuitry. A guard ring is utilised to insulate the analogue part and digital part. The top metal layer Metal-L is used as a shield to isolate noises and prevent light emission reflections. The total circuit area of this local control block is only 0.0035 mm^2, and this guarantees the miniaturisation of this optrode design.

This integral local block includes diverse components: pulse width modulator, µLED driver, pulse width modulated DAC, diagnostic sensing transistor, ΣΔ ADC and relevant supplementary elements, at the cost of only 0.0035 mm^2 die area. Owing to its neatness, all of these eighteen blocks could be shifted and distributed on the optrode shaft in future designs, to further minimise the system dimensions. Moreover, this small-scale µLED control block can be utilised to construct a high-density µLED array, and dedicated µLED drivers and data converters could be built into each individual µLED pixel channel for local optical stimulation and self-diagnosis. This could be explored in future visual prosthesis projects.

5.2.6 Chip Layout and Fabrication

The local control block depicted above has been cloned seventeen times to form both the optical stimulation subsystem and the diagnostic sensing subsystem. An 18-bit decoder is created to connect and access every µLED control & sensing block.

This optrode has been implemented and fabricated in a X-Fab 0.35-µm, 2-poly, 4-metal standard CMOS process. The global layout and micrograph of the fabricated chip are displayed in Figure 5.8. The total chip dimensions are 900 µm × 4850 µm, which fits with the proposed architecture in Figure 5.2, and a 100 µm edge is retained to provide protections for fabrication and post-processing. The dimensions

of the global logic control block are 35 µm × 570 µm, and the size of the 18 µLED control & sensing blocks is 90 µm × 900 µm. The shaft length is 4400 µm, in accordance with the six cortical layers. The shaft width is 200 µm, which contains three sections: the width of the µLED bonding pad (60 µm), the width of metal wirings and spacing (40 µm on each side), and the perimeter margin (30 µm on each side). Six µLED clusters are evenly placed along the optrode shaft, and the spacing between each two µLED clusters is 580 µm. In each µLED cluster, only a 20 µm spacing is set between each two µLEDs. This ensures that those two backup µLEDs could have a very similar penetration area to that of the main µLED. In addition, the top metal layer metal-L is retained and utilised as a shield for light reflection protection and noise isolation.

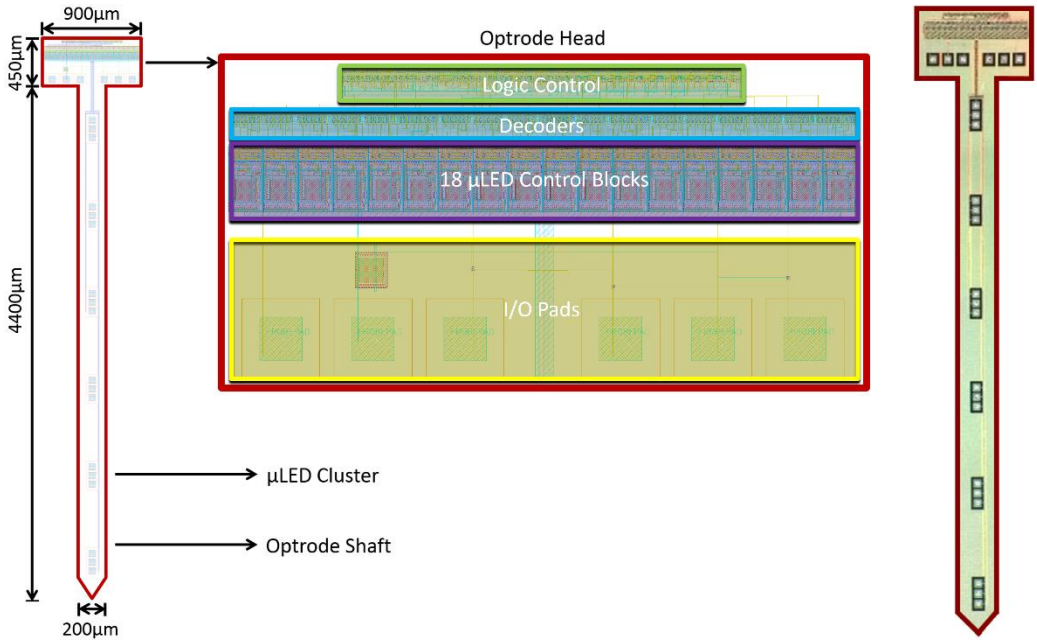


Figure 5.8 (a) Layout diagram of the open-loop optrode. Six I/O pads are used for power supply and digital & analogue I/O, with custom-designed electrostatic discharge (ESD) protection circuitry. The 18 local control blocks consume 90 µm × 900 µm die area in total. The size of the 18-bit decoder is 20 µm × 900 µm. All of these compact layouts minimise the global optrode dimensions. (b) Optrode micrograph taken from a silicon wafer.

5.2.7 Top-level Simulation Results

Stimulation Control Function

Having completed the global layout of the optrode, a top-level post-layout simulation is conducted to firstly verify the stimulation control function. In the

optical stimulation operation, the particular µLED is addressed by the global logic control module and then driven by the V_{DD_LED} with a strong current to achieve a high-intensity light delivery. During this simulation, the V_{DD_LED} is tuned from 0.0 V to 5.0 V gradually, and the current through µLED (I_{LED}) is observed. A diagram of the relationship between V_{DD_LED} and I_{LED} is illustrated in Figure 5.9. It can be observed that there is no noticeable current when V_{DD_LED} is below the µLED working threshold. When V_{DD_LED} reaches the µLED working threshold, the µLED is stimulated and an approximately linear relationship between V_{DD_LED} and I_{LED} is obtained. Furthermore, the µLED luminance can be derived from this *I-V* curve, and the correlation between V_{DD_LED} and µLED luminance is also demonstrated in the figure below. When V_{DD_LED} is over 3.5 V, the drive current would be greater than 1 mA while the luminance is reaching 100 µW. When V_{DD_LED} is equal to 5.0 V, the drive current is increased to 4.4 mA, and the corresponding luminance is 398 µW. This indicates that this stimulation circuitry could provide sufficient current to drive the µLED and deliver blue light with the targeted luminance level, as long as a voltage over 3.5 V is provided for the V_{DD_LED}.

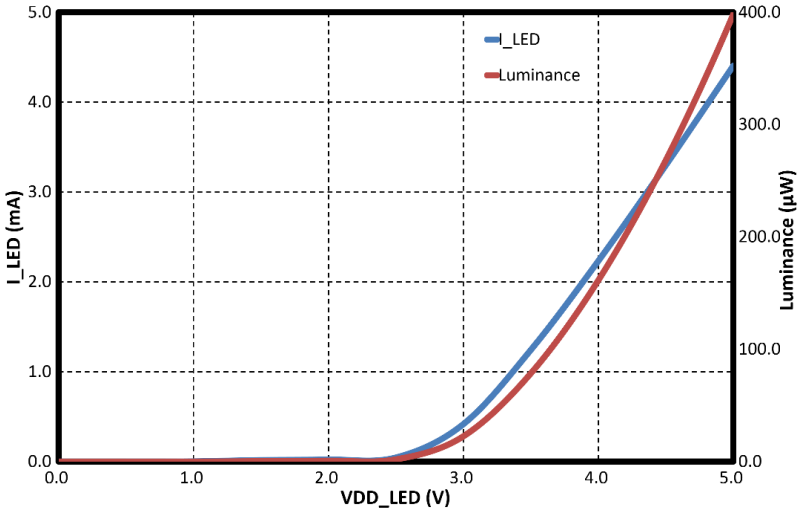


Figure 5.9 Top-level simulation results for the µLED current and luminance versus the V_{DD_LED}. The maximum value of I_{LED} is 4.4 mA, and corresponding utmost luminance is 398 µW, when V_{DD_LED} is increased to 5.0 V. Local circuit schematic is referred to Figure 5.5 (b).

Diagnostic Sensing Function

Moreover, the diagnostic sensing function is also fully validated via simulations, and Figure 5.10 illustrates the post-layout simulation results. It can be seen two µLEDs (LED_1 & LED_2) are selected to conduct comparative analysis. LED_1 is

working in the diagnosis operation state, while LED_2 maintains the off state consistently. The input *Set_Pulse* is defined as 150 ns to accomplish a 3.75 V V_{Sense} signal. During the simulation, the *Clock* signal defines the operation frequency, and the *Activate* signal controls the diagnostic sensing operation. All of the input information, which can be serially used to achieve system addressing, logic controlling, and pulse signals configuration, are transmitted via $Data_{IN}$ signal. In the output part, it can be observed that, after the PWM stage, V_{LED1} (V_{Dia1}) is equal to 2.40 V constantly, whilst V_{LED2} still maintains as 0.0 V. Moreover, at the time point of 815 ns, the 110 ns time interval of $Data_{OUT\_LED1}$ is firstly observed, whilst no valid data is observed from $Data_{OUT\_LED2}$.

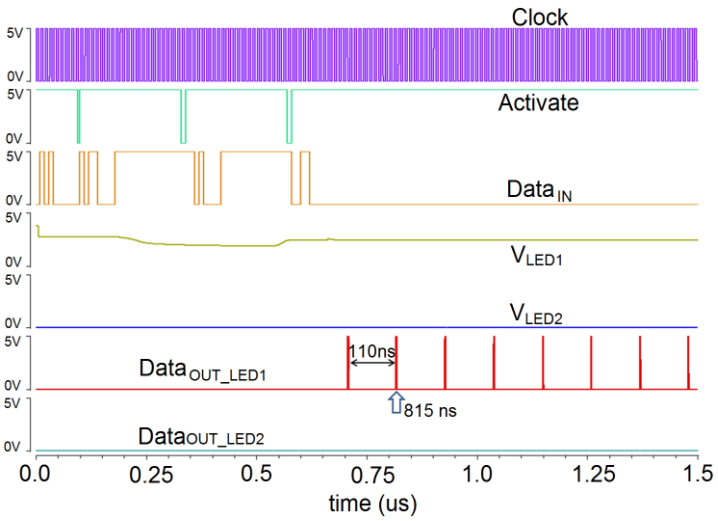


Figure 5.10 Top-level simulation results for the diagnostic sensing circuitry. A random µLED LED_1 is chosen for analysis, and LED_2 is selected for comparison. During this simulation, V_{Sense} is set as 3.75 V (e.g. $|V_{gs}|$ is equal to 1.25 V), the diagnostic voltage is equal to 2.40 V, and the $t_{interval}$ is correspondingly equal to 110 ns. Local circuit schematic is referred to Figure 5.6 (b).

In this diagnostic sensing circuit, as mentioned in Subsection 5.2.4, the V_{Sense} signal is regulated by the pulse width of the *Set_Pulse*. Then, the accuracy of V_{Sense} modulation relies on the resolution of the pulse width modulated DAC. Likewise, through the ΣΔ ADC, the subsequent V_{Dia} voltage is expressed by a pulse frequency with the time interval $t_{interval}$. The relationship curve between V_{Dia} and $t_{interval}$ is shown in Figure 5.11 below.

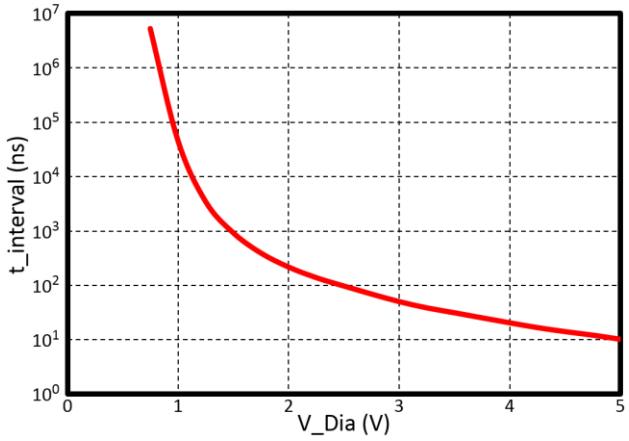
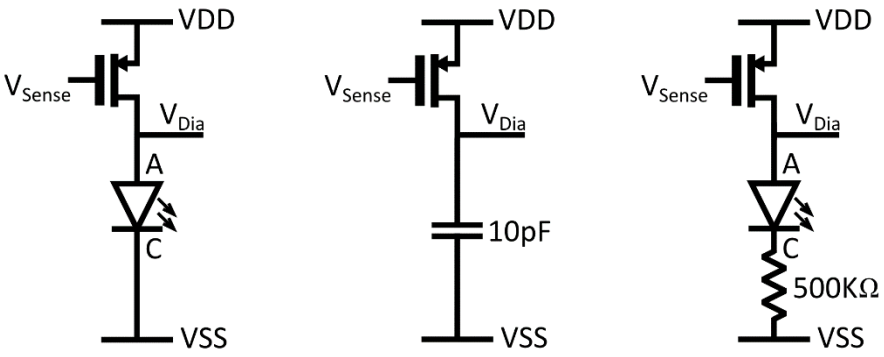
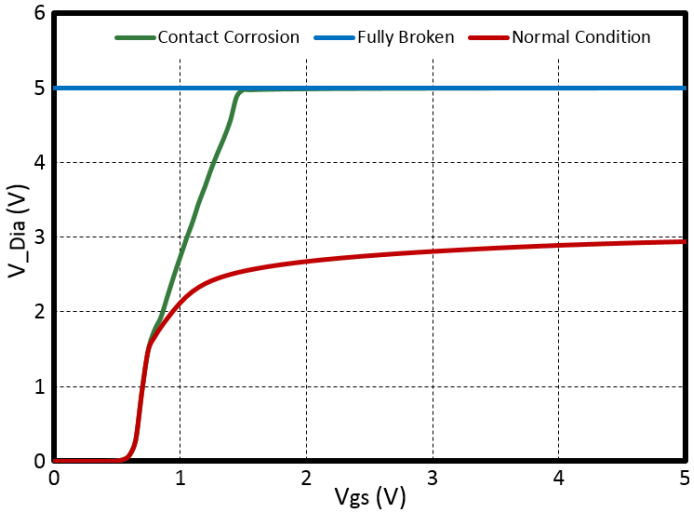


Figure 5.11 Relationship between the time intervals of output pulse versus the diagnostic voltage across µLED. The $t_{interval}$ has a vast dynamic range from nanoseconds to milliseconds, providing sufficient sampling resolution.

Furthermore, a three-state comparison simulation is conducted, and this demonstrates how V_{Dia} changes with V_{gs} in M_{diag} under different operation scenarios, as shown in Figure 5.12. The normal diode behaviour of the light emitter is represented by the red curve. Firstly, the µLED works within the transistor subthreshold region. After that, it arrives at the dark µLED sub-operating region. Finally, it arrives at the transistor saturation region. Under this condition, the sensing current I_{Dia} varies from 0 µA to 1.0 mA. In comparison, when the optrode shaft is broken, then an open circuit is formed at the stimulation site, and V_{Dia} is then equal to V_{DD_LED} and remains consistently at 5 V. To mimic this open state, a 10 pF capacitor is used to replace the µLED for simulation, and the feature curve is illustrated by the blue line. And in this situation, there is no effective current through the circuit. Alternatively, if the contact erosion happens between the active circuitry and the light emitter, the serial resistance of the µLED bonding point will be much larger, and this will be reflected by the voltage at that point. The diode behaviour will then be more resistive. Correspondingly, the effective current range is much narrower than the normal condition, and I_{Dia} is increased from 0 µA and 5.3 µA and then saturated at that value. To simulate this resistive state, a 500 KΩ resistor is serially wired with the normal µLED, and the results are illustrated by the green curve in the figure below. It can be seen that, with a predefined $|V_{gs}|$, the real-time state of the stimulation site could be fetched by observing the output diagnostic voltage. In actual applications, to avoid switching on the µLED, the targeted working range of $|V_{gs}|$ is 0-1.5 V with four sampling points. Correspondingly, the active sensing current range is 0-40 µA.



(a)



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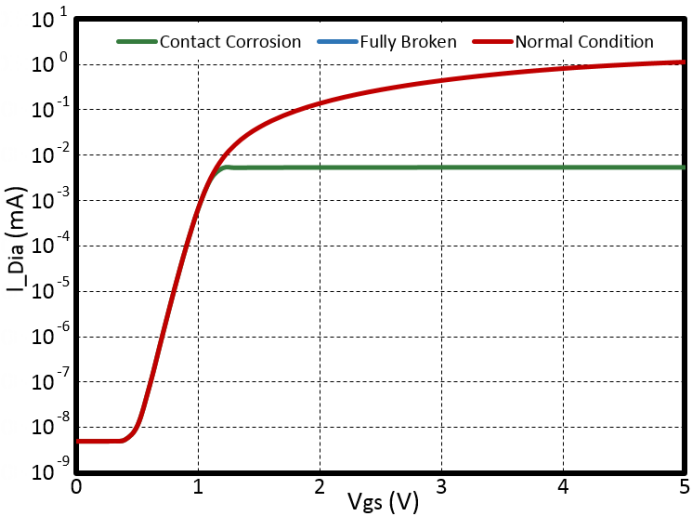
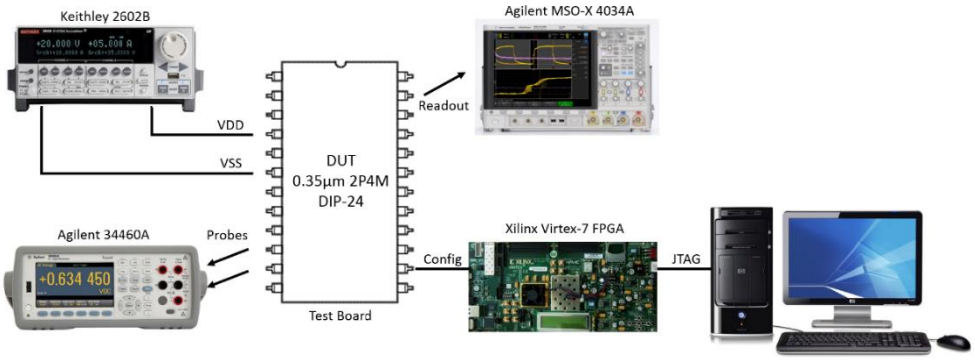


(c)

Figure 5.12 Comparison simulation results in diverse µLED operation conditions. (a) 3-condition equivalent models to represent the normal condition, optrode breakage, and contact corrosion respectively. (b) The V_{Dia}-V_{gs} feature curve. V_{gs} is the voltage difference between the gate and the source of the diagnostic transistor M_{diag}, and it is equal to $|V_{DD}$-$V_{Sense}|$. In practical usage, to prevent light emission/ccurent, V_{gs} must be below 1.5 V. (c) The I_{Dia}-V_{gs} feature curve. I_{Dia} varies from 0 µA to 40 µA when V_{gs} is in 0-1.5 V region. Local circuit schematic is referred to Figure 5.6 (b).

5.2.8 Experiment Set-up

The general testing set-up for this open-loop optrode is displayed in Figure 5.13. A Keithley 2602B source meter is utilised to provide the 5V V_{DD} and the global V_{SS}. A Xilinx Virtex-7 FPGA board is selected to configure and control the testing chip package, to support the high-frequency operation of the pulse width modulated DAC. An Agilent 34460A multimeter is used to probe and sense particular analogue signals (such as V_{LED}, and V_{Dia}), while time domain measurement is captured by an Agilent MSO-X 4034A oscilloscope.



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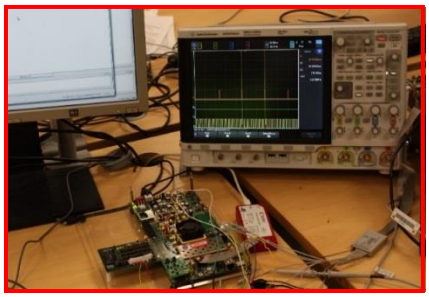


(b)

(c)

Figure 5.13 Experiment set-up. (a) General testing set-up for the open-loop optrode with room temperature 20 °C. (b) A FPGA-based testing platform, and time domain results are recorded by the high-frequency oscilloscope. (c) The µLED drive current is probed via a sensing port of the Keithley source meter. This shows that the µLED current is 4.374 mA when V_{DD_LED} is 5.0V, which exactly fits with the simulation results shown in Figure 5.9.

5.2.9 Measurement Results

Stimulation Control Function

In this part, the optrode stimulation control function has been verified on the bench after setting up the test platform. The input signals (*Clock*, *Activate* and $Data_{IN}$) are all generated from the FPGA Virtex-7 board. The primary purpose of the test is to validate the light driving ability of the proposed optrode with the tunable power

supply. A solitary Panasonic µLED is wire-connected between the LED anode pad and global V_{SS}, to measure the drive current. During the measurements, V_{DD_LED} is steadily adjusted from 0.0 V up to 5.0 V with 0.1 V steps. Measurement results are demonstrated in Figure 5.14. When V_{DD_LED} is lower than the µLED working threshold, the value of I_{LED} is at the fA or nA level. When V_{DD_LED} is above the threshold, then the light emitter is activated to perform a linear relationship between V_{DD_LED} and I_{LED}. It can be seen that, when V_{DD_LED} is equal to 5.0 V, the maximum working I_{LED} is 4.37 mA, and the corresponding effective luminance is 395 µW. These results closely match the top-level simulation results. This demonstrates that this optrode can generate sufficient luminance with high accuracy, and the targeted light delivery and penetration depth can be achieved.

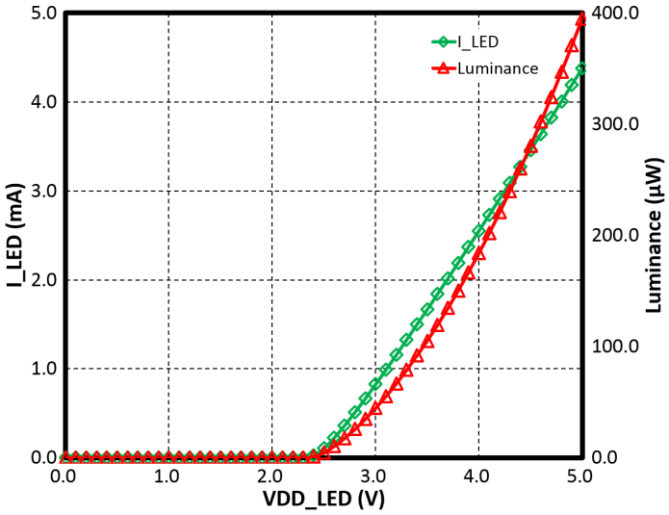


Figure 5.14 On-bench measurement results for the µLED current and luminance versus V_{DD_LED}. The maximum value of I_{LED} is 4.37 Ma, and the corresponding maximum luminance is 395 µW (deduced from Figure 3.8), when V_{DD_LED} is equal to 5.0 V. Local circuit schematic is referred to Figure 5.5 (b). Top-level simulation results are referred to Figure 5.9.

Diagnostic Sensing Function

The subsection above has verified the stimulation control function via an on-bench electrical test, and this indicates that this proposed optrode design can fulfil accurate local light emission with variable power supplies. In this part, the focus moves onto another vital criteria of this implantable optrode: safe operation. The functionality of the diagnostic sensing circuitry is then assessed using the FPGA-based test platform. Similar to the stimulation test, all the testing stimuluses for the diagnostic sensing circuitry are created by the FPGA Virtex-7 board. The *Clock* signal is set to 100 MHz to ensure a sufficient resolution of the *Set_Pulse*

signal of the pulse-modulated DAC, which could determine enough diagnosis sampling points. Global V_{DD} and V_{SS} are fixed at 5.0 V and 0.0 V respectively, using the Keithley 2602B power meter.

In order to compare the outcome with the top-level simulation results demonstrated in Subsection 5.2.7, the value of V_{Sense} is here set at 3.75 V (V_{gs} = 1.25 V) and the pulse width of the *Set_Pulse* is equal to 150 ns (both being the same as the simulation settings). Then electrical measurements are conducted, and three different optrode operation scenarios, i.e. normal operation, shaft rupture, and contact erosion condition, are validated in on-bench tests.

To test the normal operation, a fully functional Panasonic µLED is wire-connected to the µLED anode pad and global V_{SS}. When this optrode is normally running in diagnostic mode, the µLED executes like a regular diode behaviour. By defining the *Set_Pulse* input signal as 150 ns (i.e. V_{Sense} is equal to 3.75 V), the time interval $t_{interval}$ of the OUT_{Pulse} is noted as 110 ns, captured via the oscilloscope as illustrated in Figure 5.15 below. From the relationship between $t_{interval}$ versus V_{Dia} (in Figure 5.11), it can be seen that the value of V_{Dia} is 2.4 V when the $t_{interval}$ is recorded as 110 ns. This is exactly the same as the simulation result shown in Figure 5.10. Therefore, the functionality of diagnostic sensing circuit has been proven when the optrode is working normal.

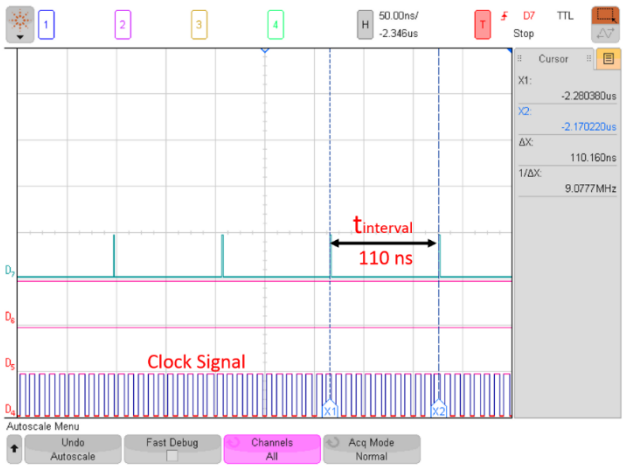


Figure 5.15 Electrical measurement results of the diagnostic sensing circuitry when the optrode operates in the normal condition. The value of the $t_{interval}$ is equal to 110 ns, matching the post-layout simulation results. Local circuit schematic is referred to Figure 5.6 (b). Simulation results are referred to Figure 5.10, Figure 5.11, and Figure 5.12.

Next, the shaft rupture situation is investigated. As explained above, when a breakage occurs in the optrode shaft, an open circuit will be created. In order to

mimic this abnormal situation, the Panasonic µLED is taken out and a 10 pF capacitor is utilised to connect to the µLED pads, to form the open-circuit situation. In this measurement, the *Set_Pulse* input signal is kept at 150 ns, and then the output signal $t_{interval}$ is recorded as 10 ns, as displayed in Figure 5.16. It can be seen from Figure 5.11 that the 10 ns $t_{interval}$ gives a value of the V_{Dia} equal to 5.0 V, and the open circuit is observed. Hence, the shaft rupture situation could be detected using this diagnostic sensing circuit.

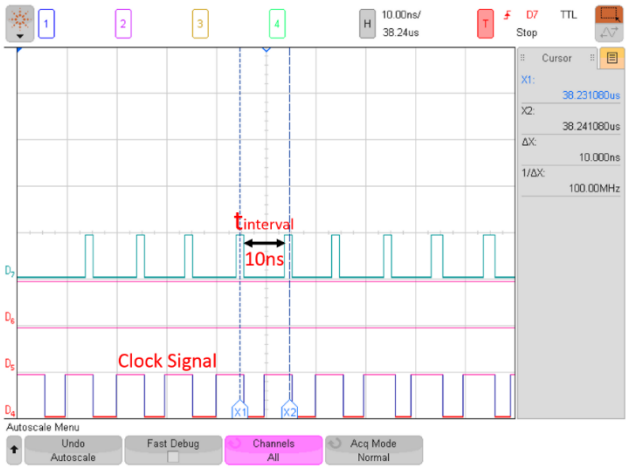


Figure 5.16 Electrical measurement results of the diagnostic sensing circuitry when the optrode operates in the shaft rupture condition. The value of $t_{interval}$ is decreased to the minimum value, 10 ns, which is the same as in the post-layout simulation result. Local circuit schematic is referred to Figure 5.6 (b). Simulation results are referred to Figure 5.10, Figure 5.11, and Figure 5.12.

Lastly, the contact corrosion situation is characterised and compared with the other two conditions. For this operation condition, as explained above, if any erosion happens at the bonding site between the CMOS circuitry and the µLED, the serial resistance will be significantly increased. Here, a 500 KΩ resistor is picked to act as the increased resistance. It is then serially connected with the Panasonic µLED to emulate the corrosion status. As the resistance of the stimulation site is higher than expected, it could be reflected and extracted by the V_{Dia}. In this measurement, all the parameter settings are kept same, i.e. 100 MHz *Clock* and 150 ns *Set_Pulse*. The output pulses are caught by the oscilloscope and depicted in Figure 5.17. It can be observed that $t_{interval}$ declines to 60 ns rather than the normal value of 110 ns (shown in Figure 5.15). This is because of the increased sheet resistance and the corresponding higher diagnostic voltage V_{Dia}, which results in a shorter $t_{interval}$ expression. Based on the $t_{interval}$-V_{Dia} relationship shown in Figure 5.11, this V_{Dia} is

decoded as 3.5 V, which perfectly matches the preceding analysis. Thus, the diagnostic sensing circuitry has also been proven with the bonding corrosion status.

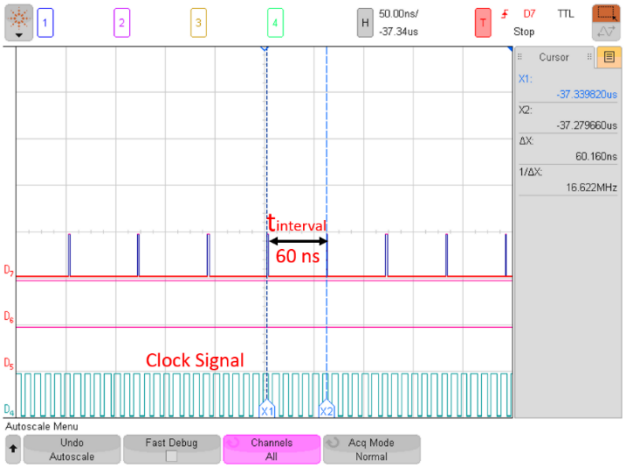


Figure 5.17 Electrical measurement results of the diagnostic sensing circuitry when the optrode operates in the contact corrosion condition. The value of $t_{interval}$ is fixed at 60 ns, as in the post-layout simulation result. Local circuit schematic is referred to Figure 5.6 (b). Simulation results are referred to Figure 5.10, Figure 5.11, and Figure 5.12.

Thus by repeating the measurements conducted above with other sampling points (V_{gs} = 1.5 V, 1.0 V, and 0.75 V), the comparison measurement results of the three-state operations are obtained and matched with the simulation results, as shown in Figure 5.18. In summary, through these comparative measurements, three different optrode operation situations can be distinguished by the diagnostic sensing circuitry. The real-time working condition of this optrode could then be identified, and any breakage or corrosion can be detected.

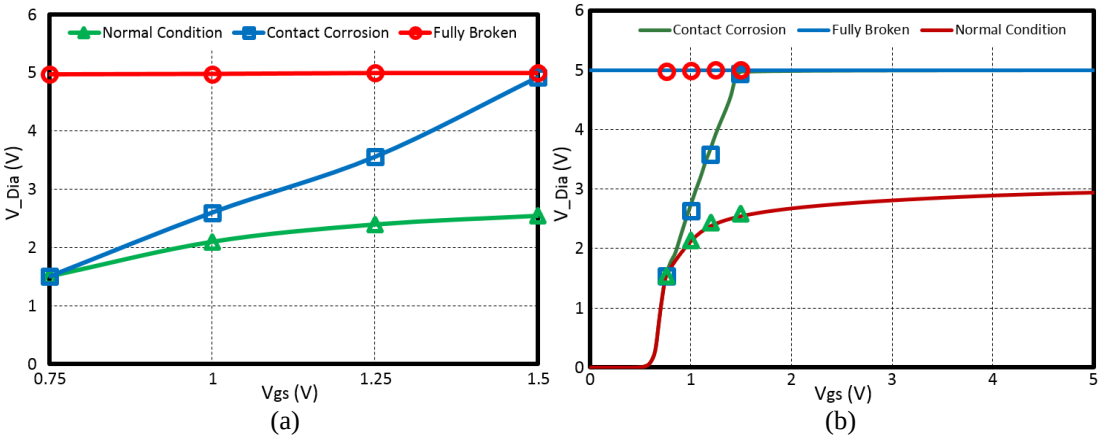


Figure 5.18 (a) Comparison measurement results of three-state μLED operation conditions. The green curve represents the normal operation state; when V_{gs} is defined as 0.75 V, 1.0 V, 1.25 V and 1.5 V, the normal V_{Dia} varies from 1.5 V to 2.5 V. The blue curve demonstrates the contact corrosion state; with same sampling points, the resistive V_{Dia} is increased from 1.5 V up to 5 V. The red line expresses the optrode rupture status; the V_{Dia} is equal to 5 V constantly. (b) Measurement results overlay with the simulation results in Figure 5.12 (b). Local circuit schematic is referred to Figure 5.6 (b).

Power Consumption

Based on all the simulation and measurement results (with room temperature 20 °C) previously obtained, the system power consumption of this open-loop optrode is calculated and summarised in Table 5.1. It can be seen that the total power consumption of the optrode is 1.008 mW when only one µLED is turned on at the same time. In particular, the light power consumes the majority of the system power (1.005 mW, 99.7%). As defined in Chapter 3, Section 3.9, the power budget provided by the battery is 14 mW and the continuous light power is 13 mW. Thus, in actual use, at least twelve µLEDs can be simultaneously turned on in the single optrode, or multiple optrodes (up to twelve) can be manipulated at the same time if only one specific µLED needs to be activated.

Table 5.1 Total power consumption of the open-loop optrode.

Subsystem	**Major Circuits**	**Static power (µW)**	**Dynamic power (µW)**	**Utilised circuits duty cycle**	**Total Power (µW)**
Logic control	Logic control	0.00	2	100%	2
Optical stimulation	Pulse width modulator	0.00	1.28×10^{-3}	100%	1.28×10^{-3}
	Logic cells	0.00	1.06×10^{-3}	100%	1.06×10^{-3}
	µLED	2.01×10^{4}		5%	1005
Diagnostic sensing	Pulse modulated DAC	5.77×10^{-6}	8.45	1%	0.0845
	Sensing transistor	100		1%	1
	ΣΔ ADC	3.3×10^{-6}	12.6	1%	0.126
Total Power (µW)		1008.21			

Although this design meets the system power requirement, there are still some space for optimisations, to ensure the minimal consumption. Lower-power designs and power-gating strategy would be explored in future designs.

5.2.10 Summary

In the previous subsections, the functionalities of this open-loop optrode design have been fully validated both in simulation and on-bench tests with the expected results. Table 5.2 summarises the overall system performance of this optrode.

Table 5.2 Performance summary of the open-loop optrode.

System Overview	
Technology	0.35-µm, 2-poly, 4-metal X-Fab CMOS process
Operation voltage	3.5 - 5.0 V
Active circuits area	0.13 mm^2
Total Power	1.01 mW (1 µLED)/6.04 mW (6 µLEDs)
Optrode head dimensions	1000 µm × 450 µm
Optrode shaft dimensions	4400 µm × 200 µm
No. Stimulation sites	6
No. µLEDs	18
Optical Stimulation	
µLED current range	0 - 4.37 mA
Maximum luminance	395 µW
Maximum light intensity	1256 mW/mm^2
Stimulation mode	Mono-direction
Modulation methods	PWM
Diagnostic Sensing	
No. sampling points (Min)	4
Sampling rate (Max)	100 MHz
Input sensing current	0 - 40 µA
Output diagnostic voltage	0 - 5.0 V

In this section, the first version of the proposed optrode is developed and fabricated in standard 0.35-µm CMOS process. Multi-site stimulation and targeted light delivery are realised, with sufficient light luminance. The µLED clustering structure is constructed to realise a backup mechanism, significantly enhancing the optrode durability and robustness. A PWM scheme is utilised to programme the light intensity. This not only ensures light emission efficiency but also regulates the thermal effects associated with the light emitters. Moreover, a self-diagnosis function is developed to monitor the optrode working status in real-time. If any abnormality occurs, either substrate breakage or µLED bonding erosion, it can be observed by the

diagnostic sensing circuitry. Based on different scenarios, this will let user/clinical technician decide whether to switch to a backup µLED or to entirely turn off the implant. This self-diagnosis strategy profoundly enhances the functioning reliability and operational safety of the proposed optrode.

Although this optrode design has met the demands for local light delivery and safety evaluation, there are still several limitations which need to be highlighted here and taken into account in future designs. One point is limited light intensity controllability. PWM is included into this optrode, making the light intensity tuneable, and the power supply of µLED drive circuits could also be adjusted (from 3.5 V to 5.0 V) to generate variable levels of drive current. Even though these two methods could programme driving ability to some degree, stimulation current/light intensity cannot be directly and accurately controlled. Besides, as described previously, an appropriate stimulation current is vital for both tissue health and thermal effects. It is desirable and critical to create a direct current/light intensity control strategy, further optimising luminance controllability. This can not only improve the stimulation efficiency, but could also benefit system safety and stability. Moreover, this optrode has realised the self-diagnosis function for the first time. This sensing scheme ensures system reliability. But, in applying this particular pulse modulated DAC, high operational frequency is needed, and only limited sampling points are obtained. In the future, lower-frequency data converters need to be incorporated to obtain a higher-resolution diagnosis. Furthermore, the thermal effects of light emissions into surrounding tissues should be carefully investigated. Although the PWM could control local intensity, and then to adjust heating dissipation to some extent, there is a necessity to build a dedicated temperature sensing circuitry to monitor the thermal effects with light emitters. This would be beneficial for both electronics stability and patient health. Finally, there is an increasing need to integrate external electrical neural recording into the optogenetic implant. This could provide real-time feedback neural signals for the optical stimulator, to determine corresponding actions. An optical-electro neural stimulation-recording system should then be constructed for closed-loop neuroprosthesis applications.

5.3 Closed-Loop Optrode for Optical Neural Stimulation and Electrical Neural Recording

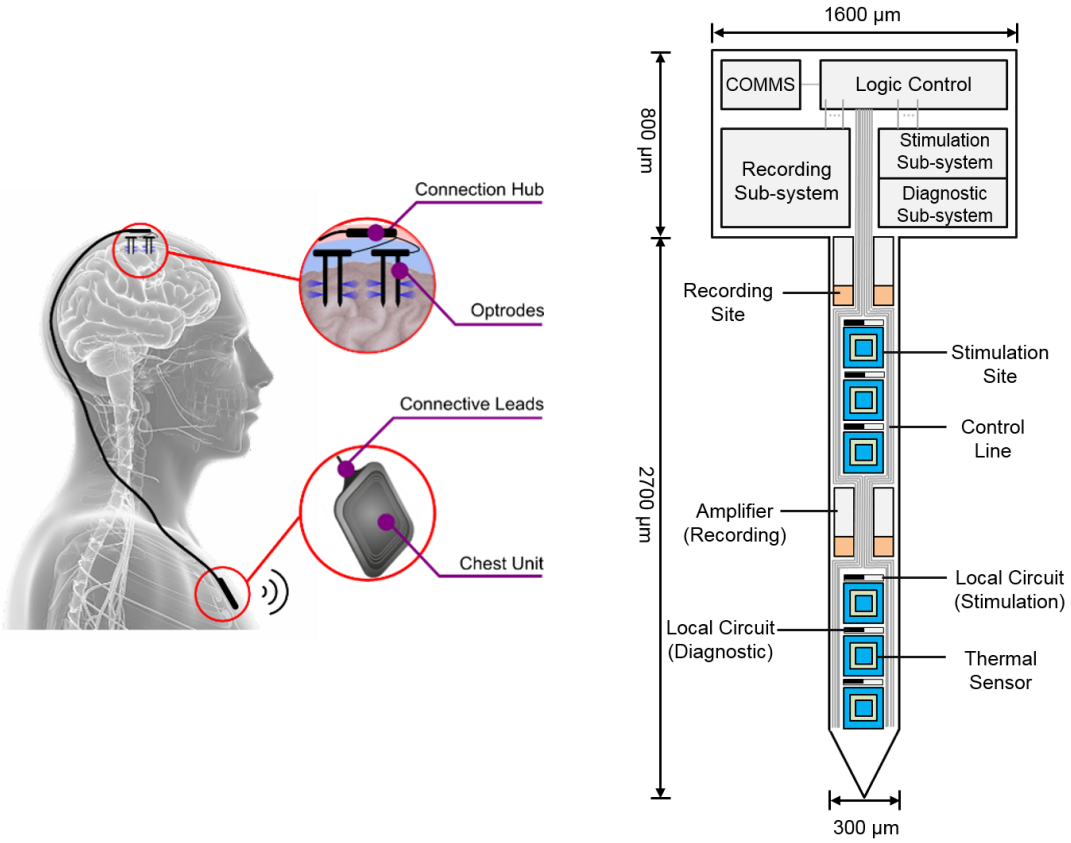
In the previous section, the first-version CMOS-driven optogenetic implant has been developed. It is capable of controlling light emission for multi-site stimulation. In particular, the PWM scheme is created to regulate the luminance. In this section, an intensity magnitude modulation method is formed along with the PWM. This is accomplished by tuning the drive current of the μLED via an 8-bit DAC, which could produce more-accurate light intensity modulation. Moreover, a biphasic μLED driver is designed for optical neural stimulation for the first time. This would benefit both current optrodes and future explorations.

As highlighted before, since the optical probe (including the light emitters) would be imbedded into the human brain, it is important to carefully consider the circuitry reliability and long-term durability. A potential danger which may arise during device implantation is shaft rupture. Another hazard is contact erosion at the μLED bonding sites. To manage both risks, the diagnostic sensing circuitry is retained and updated within this new optrode. In particular, 8-bit data converters are utilised to fulfil a high-resolution diagnosis function. Also a dedicated TCA is developed to further restrain the sensing current within a highly safe region.

In order to further guarantee circuitry robustness and patient health, thermal sensing circuitry is built into this optrode. Resistor-based temperature sensors are placed close to each stimulation point which could monitor the thermal effects associated with the μLEDs.

When the targeted neurons are photosensitized by blue light, it would be meaningful to monitor the local neural activities in the vicinity of stimulation sites. Local Field Potential (LFP) recording circuits which were developed by my collaborators [123, 124] are therefore included in this newly proposed optrode, accomplishing an optical-electro closed-loop neural interface. Figure 5.19 shows the system architecture of this optrode and demonstrates how this optrode concept will be utilised with a chest unit for implantable neuroprosthetics.

5.3.1 System Architecture



(a) (b)

Figure 5.19 (a) Proposed optrode for both optogenetic stimulation and electrical recording. The optrode will communicate with a chest processing unit for closed-loop processing. (b) The design floorplan of the optrode displays the arrangement of the different subsystems. The optrode head area is defined as 800 µm × 1600 µm to contain the majority of circuit designs. The width of the optrode shaft is increased to 300 µm to include the local circuitry on the optrode shaft.

This subsection describes the system architecture of this multi-functional closed-loop neural implant, as demonstrated in Figure 5.19 (b). This optrode contains four sub-systems: optical stimulation subsystem, diagnostic sensing subsystem, LFP recording subsystem and logic control subsystem. The area of the optrode head part is initially defined as 800 µm × 1600 µm, and it contains all of the global circuits of these four subsystems. This dimensions can be adjusted based on different configurations. The width of the optrode shaft is extended to 300 µm, which provides dedicated space for local circuits on the shaft. Two clusters of stimulation and recording sites are uniformly distributed along the 2.7mm-long optrode shaft. Each cluster has three optical stimulation sites (with in-built diagnostic sensing circuits), and two electrical recording sites. This clustering configuration affords suitable

positioning and redundancy of functioning elements. Local CMOS circuitry is implemented at the vicinity of each stimulation site and recording site, and this allows for precise local light delivery, accurate low-noise neural recording and sensitive real-time self-diagnosis & thermal sensing. The total length of the current optrode is 3.5 mm long, and it can be extended to 6 mm, with additional stimulation and recording clusters.

In the optical stimulation subsystem, PWM and intensity magnitude control electronics are both utilised to achieve advanced overall light intensity modulation. Six stimulation sites are built along the optrode shaft to produce local light emission at different depths. A biphasic µLED driver is realised in each local stimulation control block to obtain bidirectional stimulation, which can benefit both light emission and diagnostic sensing and also would be useful for future designs.

Moreover, diagnostic sensing electronics are also built into the optrode to evaluate its operational functionality. At each stimulation site, local diagnostic sensing circuits are implemented alongside the stimulation blocks. Abnormalities could then be detected by this diagnostic sensing scheme if there is an optrode shaft breakage or a degradation of the µLED bonding sites. This would determine the system operation stability and long-term durability.

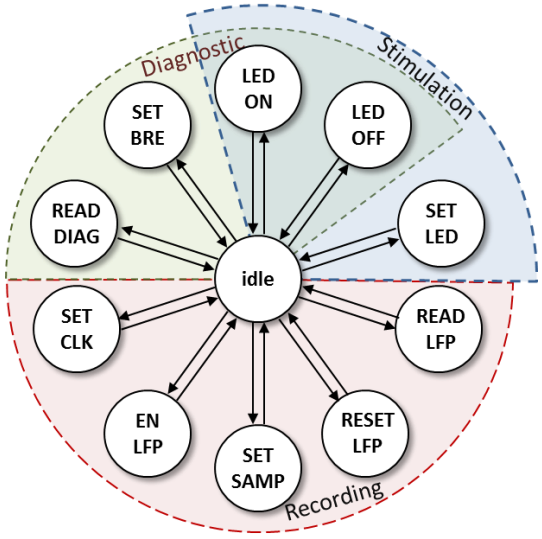
Furthermore, a local temperature sensing structure is also developed to investigate the opto-thermal effects of light emitters. This would prevent both circuitry degradation and tissue damage caused by light heating. Besides, the neural recording system is adapted and implemented to record in-situ LFPs, then to form a feedback system with the optical stimulation electronics. At last, a SPI bus is implemented to provide logic command interpretation, and a finite state machine (FSM) is realised to address and control the operations of each subsystem.

5.3.2 Logic Control

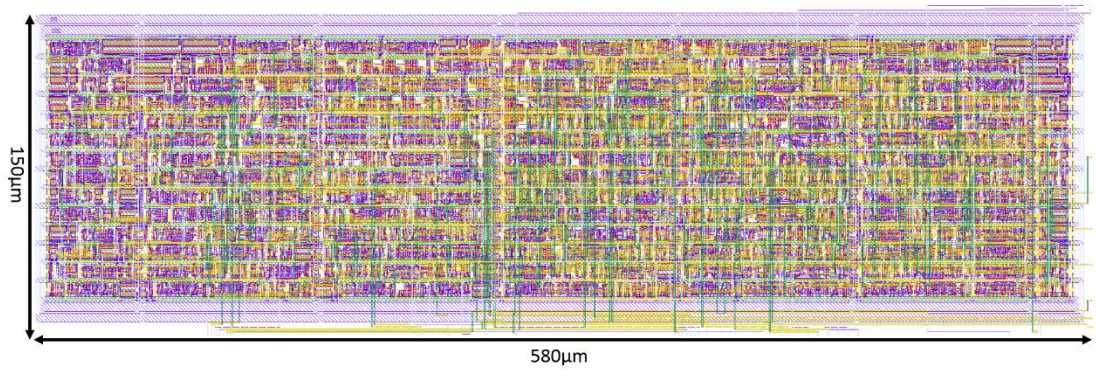
In the logic control subsystem, a SPI-based command interpreter is generated to fetch external commands and perform corresponding operations, and a FSM is designed to realise this logic control scheme. The FSM receives the SPI commands and subsequent input data from the master (either a microcontroller or FPGA). After that, corresponding control signals are generated and sent to the different subsystems

and sub-blocks, and related output data are then fetched upon request. In particular, the SPI transceiver is controlled by a dedicated SPI clock (MCLK), whereas a master clock signal is set to synchronise all the operations of this optrode, which ensures the timing accuracy and operation stability. Additionally, an external global reset is reserved which could reset all internal states in case of any fault being observed, and all optrode operations would then be shut down.

Figure 5.20 depicts all FSM states and corresponding transition conditions, showing the ten different operation states for the three subsystems. Specially, *Set_LED, LED_ON and LED_OFF* are responsible for light emission operations. The *Set_LED* defines the input of the stimulation DAC, and then the value of stimulation control voltage $V_{Control}$ and drive current I_{LED} are determined. This accomplishes the intensity magnitude modulation. *LED_ON* and *LED_OFF* define the operation state of the particular µLED and maintain the current status until a new working state is updated upon request, and these signals are in charge of the PWM control of light emissions. The *Set_Bre* and *Read_Diag* are the two main commands for the diagnostic sensing subsystem. The *Set_Bre* enables the diagnostic DAC and also defines the input values to sweep the sensing current from 0 µA to 11 µA. The *Read_Diag* command is then executed to extract and transmit the diagnosis voltage. The other six states are dedicated for LFP recording operations, and are not detailed here. Further information can be obtained elsewhere [134].



(a)



(b)

Figure 5.20. (a) Command trees of the FSM states and corresponding transition conditions. (b) Layout of the FSM, implemented in the digital design flow.

5.3.3 Stimulation Control Subsystem

The stimulation control subsystem primarily contains six individual stimulation sites along with the corresponding local control circuits. Each local control block consists of three main parts: intensity magnitude modulation module, pulse width modulator and biphasic µLED driver (H-Bridge). In the intensity modulation module, a common 8-bit resistor string DAC and a multiplexed 3.3 V-to-5 V Inverting Voltage Amplifier are utilised for setting the stimulation control voltage $V_{Control}$ of each µLED driver. By adjusting the value of $V_{Control}$, the current level through each µLED could be modulated with high resolution. A schematic diagram of this optical stimulation circuitry is illustrated in Figure 5.21.

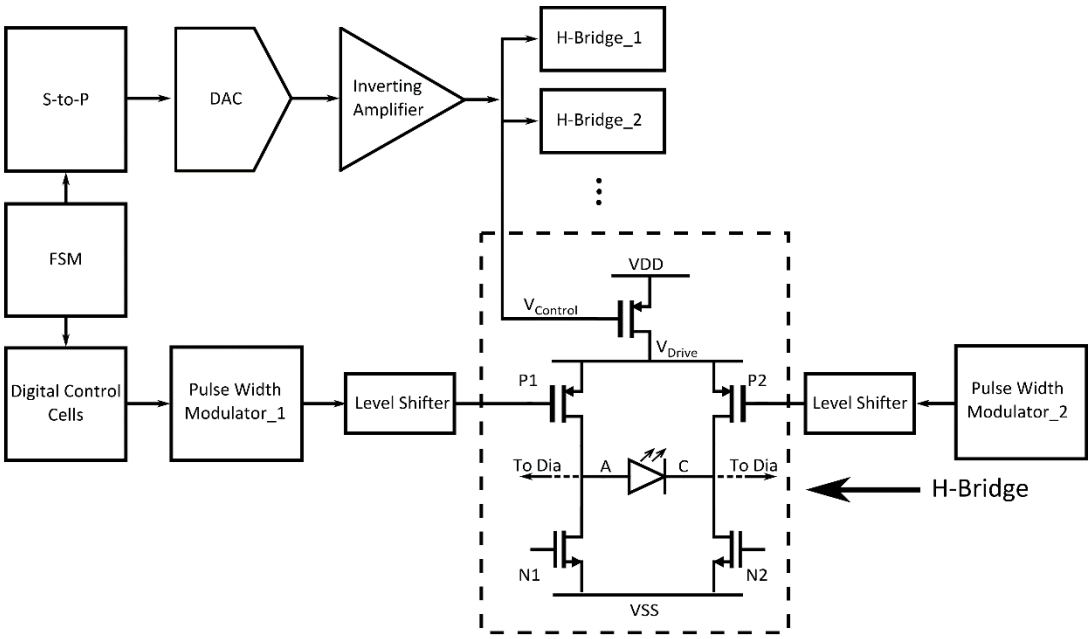


Figure 5.21 Schematic diagram of the optical stimulation circuitry. I_{Drive} is the µLED drive current created via the DAC and TCA, and it then go through the µLED via P_1 and N_2. A H-Bridge, which is adopted from Chapter 4, Section 4.2.2.3, is utilised for µLED emissions. Within the H-bridge module, the anode and cathode of each µLED are also linked to the diagnostic sensing circuit. In this design, the DAC module is described in Chapter 4, Subsection 4.2.6.1, and the Inverting Voltage Amplifier in Chapter 4, Subsection 4.2.5, the pulse width modulator in Chapter 4, Subsection 4.2.4.2, the S-to-P in Chapter 4, Subsection 4.2.7, and the level shifter in Chapter 4, Subsection 4.2.8.

The pulse width modulator primarily contains two D-Latches and additional logic units. The local memory units and logic cells receive external commands and data from the FSM. This information is then decoded into corresponding operation indexes to achieve three different working modes: off, stimulation and diagnostic. The pulse width modulator could then be switched with particular frequencies to PWM control if the light emitter is operated in the stimulation mode. A H-Bridge configuration is formed in the µLED drive part to attain biphasic light emissions. This structure would also be employed to analyse the electrical features of the reverse-biased µLEDs. This H-Bridge configuration could also avoid the possibility of degeneration by the electric field between the µLED anode and the common ground. This H-Bridge structure could be configured for both µLED stimulations and diagnostic sensing, via the memory units and logic cells at the pulse width modulator part. The function table of the H-Bridge configuration is shown in Table 5.3. It can be observed that different operations can be performed: Forward Stimulation, Reverse Stimulation, Forward Diagnostic and Reverse Diagnostic.

Table 5.3 Truth table of H-Bridge control signals.

Control Signals				**Function**
P_1	P_2	N_1	N_2	
0	1	0	1	Forward Stimulation
1	0	1	0	Reverse Stimulation
1	1	0	1	Forward Diagnostic
1	1	1	0	Reverse Diagnostic

5.3.4 Diagnostic Sensing Subsystem

Since the optrode would be inserted into the human brain, it is essential to detect any operational degradation of the optrode, particularly at stimulation points, to prevent any unexpected stimulation current being injected into the tissue. When the optrode is normally operated, the light emitter demonstrates a regular diode *I-V* feature. But, when some abnormalities occur in the optrode, such as the substrate breakage or µLED bonding erosion, this behaviour will obviously differ from the normal profile. These abnormalities could be observed by sweeping the current through each stimulation site and then extracting the subsequent voltage profiles. For instance, if the contact corrosion appears, then the serial resistance of the µLED will be dramatically increased, which will make the µLED feature curve more linear and the voltage across µLED will be higher than normal value. Alternatively, if mechanical breakage happens, an open circuit will consequently be formed, and this can be reflected in the voltage at that point.

Thus, the proposed diagnostic sensing circuit is implemented to identify these two abnormal conditions, and the system diagram is shown in Figure 5.22. In this circuit, the 8-bit resistor string DAC is selected to set the input voltage. Then a step-up TCA is incorporated to convert the input voltage into the sensing current I_{Dia}, to obtain the µLED current scanning. Since it is not desired to turn on the µLED during the diagnostic sensing stage, the I_{Dia} is limited to the 0-11 µA range by the TCA, so as to operate safely. It is then pushed into the µLED driver (H-Bridge) through an analogue DEMUX to sense a particular µLED (via the µLED address, LED_n). By sweeping the I_{Dia} via adjusting the 8-bit DAC inputs, the profile of the diagnostic

voltage V_{Dia} is then created across the µLED. Consequently, this output voltage could then be extracted and transmitted to an 8-bit SAR ADC via an analogue MUX. By tracing these diagnostic output voltages, the operation conditions of the light emitters can be monitored in real-time. Notably, this diagnostic sensing circuit is connected to the H-Bridge to execute two-mode bidirectional diagnostic sensing: forward diagnostic and reverse diagnostic. The forward diagnostic operation is carried out to achieve the regular self-diagnostic function, and the reverse diagnostic function can be utilised to explore interesting characteristics (such as current-temperature linearity) of the reverse-biased µLED for future designs.

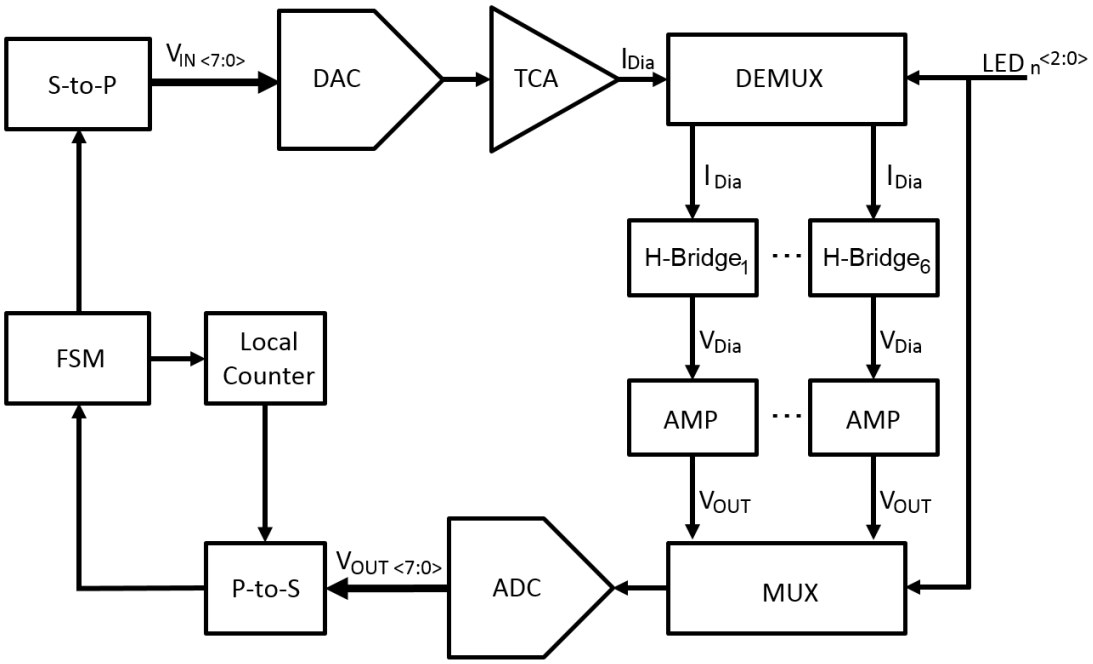


Figure 5.22 Block diagram of the diagnostic sensing circuit. It consists of DAC module, TCA module, analogue DEMUX & MUX, shared H-Bridge, ADC module and supplementary cells (S-to-P, P-to-S, and local counter). The diagnostic sensing circuit receives global commands from the FSM. A local counter is utilised for the timing control of the ADC readout. The DAC module is described in Chapter 4, Subsection 4.2.6.1, the TCA in Chapter 4, Subsection 4.3.2, the ADC in Chapter 4, Subsection 4.3.3.1, and the S-to-P and P-to-S in Chapter 4, Subsection 4.2.7 and 4.3.4 respectively.

5.3.5 Local Block Integration

The previous two subsections have described the structures and verified the performance of the optical stimulation circuitry and diagnostic sensing circuitry. This part describes how the stimulation function and the diagnostic function are integrated and implemented into each local µLED control & sensing block.

In the stimulation circuitry, the DAC, Inverting Voltage Amplifier, and S-to-P interface are utilised as common components and multiplexed by six stimulation sites. However, the H-Bridge, Pulse Width Modulator, Level Shifter, and accessory logic cells are placed next to each stimulation site to achieve individually direct stimulation control. Similarly, for the diagnostic sensing circuitry, the DAC, ADC, TCA, S-to-P and P-to-S are shared by all diagnostic channels, while local sensing elements are allocated close to each stimulation site to monitor the operational state in the vicinity. As every µLED point performs both stimulation and diagnostic functions locally, it is sensible to integrate these two types of local circuits into a compact and integral functioning block. This diminishes the cost of circuit area, reduces the efforts of wire connections, and simplifies the working load of the logic control. The layout of the integrated stimulation-diagnostic local block is implemented as illustrated in Figure 5.23.

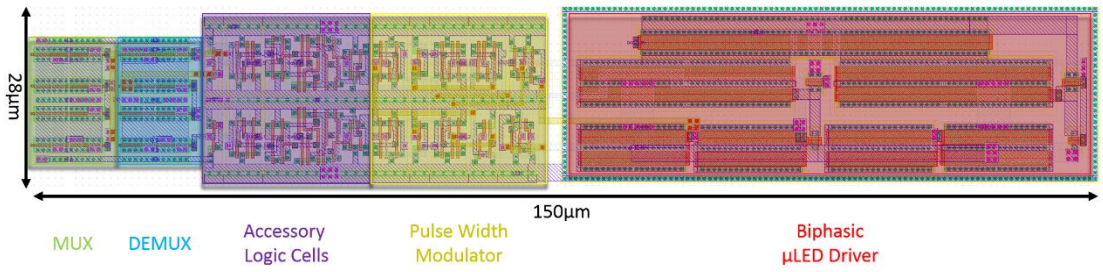


Figure 5.23 Layout of the integrated local µLED control & sensing circuitry. A guard ring is utilised to isolate the µLED drive circuitry from digital elements. The top metal layer Metal-4 is used as a shield for noise isolation and light reflection protection. The total circuit area of this µLED local control & sensing block is only 0.0042 mm^2, ensuring the miniaturisation of this optrode design.

It can be seen from Figure 5.23 above that the size of this local control block is only 28 µm × 150 µm, and this compact layout makes the localisation of each µLED control & sensing block possible. In Section 5.2, eighteen µLED control & sensing blocks built in the first-version optrode were all placed in the optrode head. In the current version, each block is moved from the head to the optrode shaft, which makes fuller use of the chip area and further optimises the optrode dimension. This integrated local block is repeated six-fold, and all six blocks are fitted into the 300µm-wide optrode shaft for direct multi-site/multi-layer operations.

5.3.6 Temperature Sensor

The subsections above explains the accomplishment of optical stimulation function and diagnostic sensing function, and provide a sound basis for the construction of this new CMOS-driven µLED optogenetic implant. However, heating is always a key concern in this direct µLED-on-optrode approach. Thermal effects during µLED stimulation are critical for both circuit operation and tissue health. It is thus essential to measure the temperature near the µLED. Hence, a simple resistor-based in-situ temperature sensor is proposed here, and the circuit diagram is shown in Figure 5.24. This sensing circuit is mainly based on exploiting temperature coefficient of the metal resistance. The resistor sensing core has been implemented as a spiral coil using the Metal4 layer (W = 0.6 µm, L = 3100 µm) with a nominal resistance of 220 Ω. Using a voltage bias (on one terminal of the resistor), and then the signal change due to temperature variation can be detected using a basic amplifier.

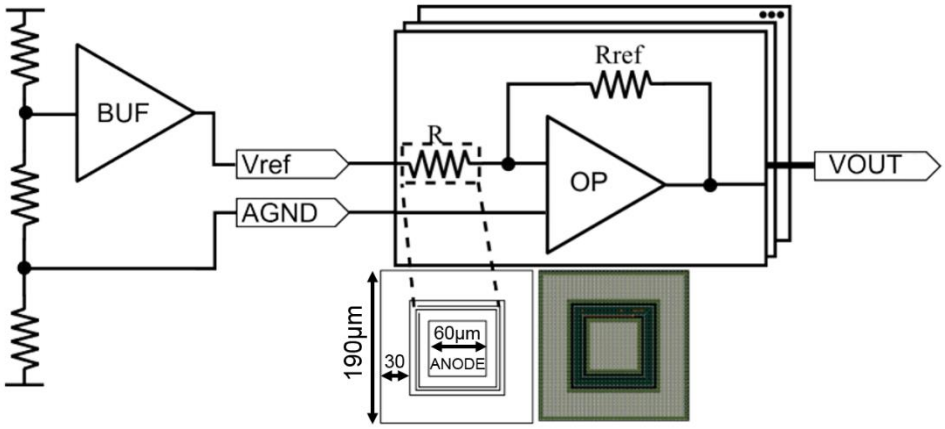


Figure 5.24 Circuit schematic of the temperature sensor. This design is positioned in the gap between the µLED anode and cathode. The µLED pads include a pad ring for the cathode, and a square centre pad for the anode. This pad configuration is chosen to achieve reliable thermal measurement, and it is also beneficial in achieving bi-direction stimulation. The buffer and operational amplifier used here are adopted from Dr Yan Liu's previous work in [134].

To accommodate the above mentioned interface within the optrode, the resistive sensing cores are placed underneath the µLED pads along the optrode shaft, while the sensing circuits are positioned on the optrode head. Metal tracks connect the cores and amplifiers, with a resistance 1/5- 1/7 of the sensor resistance. This thermal sensor could monitor the heating effect at each µLED, and it further enhances the system functioning safety and operational reliability.

5.3.7 Neural Recording Subsystem (Dr Yan Liu's Work)

As mentioned before, it is very meaningful to import the neural recording circuitry into the optrode to monitor the LFP activities, so as to obtain simultaneous feedback recording in situ and to accomplish closed-loop neural modulation.

In general, the amplitude of LEP signals is approximately 5-10 mV, and the typical power spectrum is below 100 Hz. Figure 5.25 displays the schematic diagram of the proposed LFP neural recording system. It primarily contains three parts: four local recording channels, a common SAR ADC, and accessory logic cells. A capacitive-coupled low noise amplifier (LNA) and a subsequent 2nd gain stage are built into every recording channel to amplify the small input signal, and this allows for making full use of the ADC dynamic range. The output from local channels is recognised by an analogue MUX and then transmitted into the ADC via a voltage buffer. By employing this LFP recording circuitry, local neural signals could be observed, and feedback information could be provided to the stimulation operations.

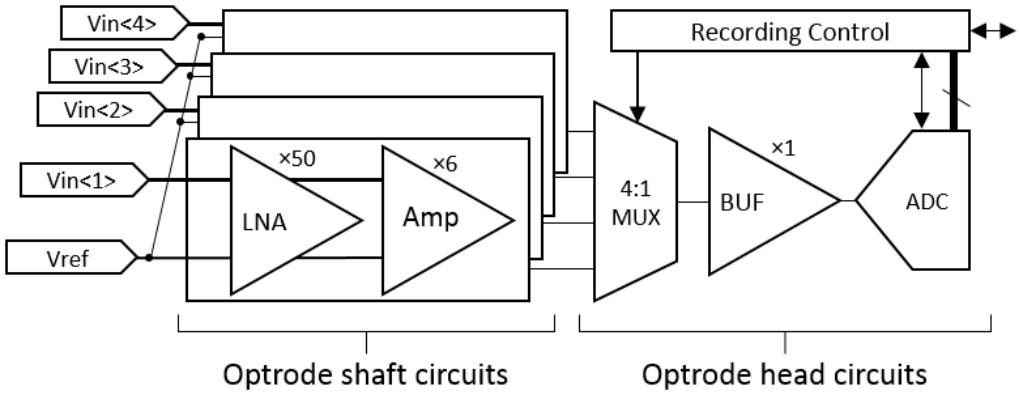


Figure 5.25 Schematic diagram of the electrical neural recording subsystem. The LNA design is adapted from [135]. It is applied to couple with the recording microelectrodes to afford low-noise amplification, and further amplification is achieved by utilising a 2nd-stage amplifier. The two-stage amplified signals are then recorded by the ADC module. This work was conducted by my colleague, Dr Yan Liu.

5.3.8 Configurations - Active Optrode and Passive Optrode

In the previous subsections, all of the major circuitries in this optrode design have been presented. This subsection describes how the proposed optrode is constructed using these developed circuitries. Two different configurations have been explored: an active controlling structure and a passive controlling structure. Although the focus of this thesis is to develop an active control optogenetic implant, it is straightforward

to convert existing circuitry and subsystems into a passive configuration for wider exploration. The floorplans of both active and passive optodes are demonstrated in Figure 5.26 below.

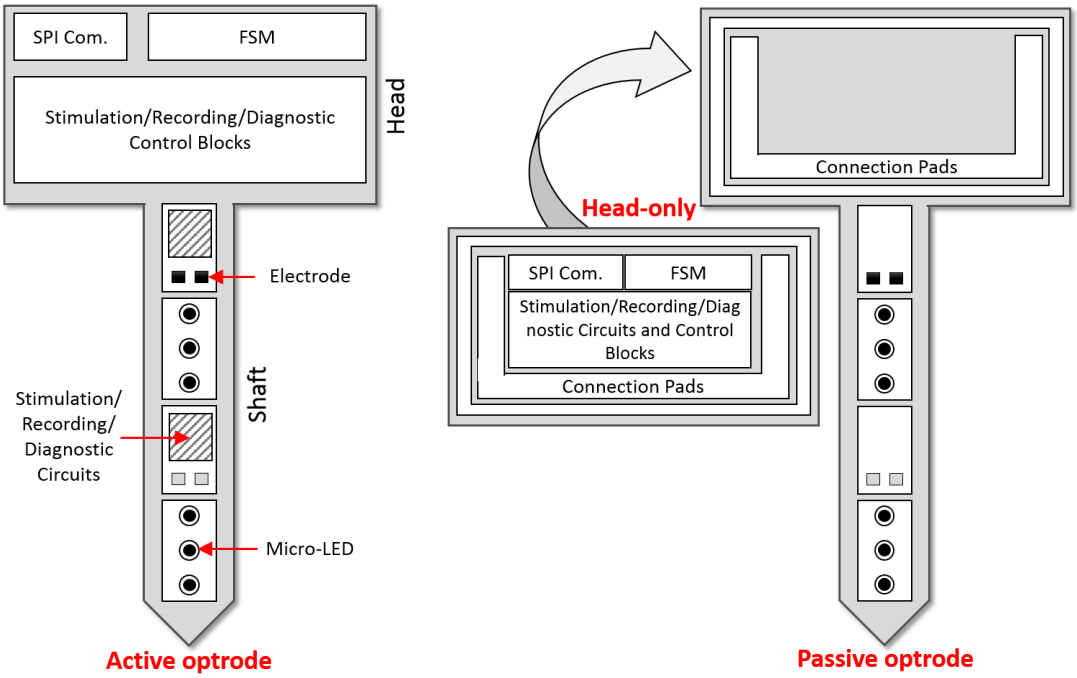


Figure 5.26 (a) Floorplan of the active optrode. All local µLED control & sensing circuits are distributed along the optrode shaft alongside the recording circuits, while common components are multiplexed and placed at the head part. (b) Floorplan of the passive optrode. This includes two parts: the T-shape passive frame with both stimulation and recording pads, and the optrode patch (head-only) which contains all the functioning circuitry of the optrode.

Active Optrode

In the active optrode, the functioning circuitry is placed in both the optrode head and the shaft, matching the system architecture proposed in Figure 5.19. Individual µLED control & sensing blocks are positioned along the shaft, to accomplish the local control of each light emitter. And local degradation & thermal sensing and simultaneous neural signal monitoring could be also achieved. The shared components, including the DAC, ADC, S-to-P, P-to-S, Inverting Voltage Amplifier and TCA, are located at the head of the optrode along with the FSM module. This active configuration makes full use of the die area. It also ensures the system integrity of the optrode. After fabrication, the active optrode only needs to be cut out as an integral T-shape, and no additional bonding stage is required.

Passive Optrode

The passive version primarily consists of two portions. One is the T-shape passive frame, in which there is no functioning circuitry. Six µLED bonding pads and four microelectrode sites are distributed on the shaft of the passive frame. Besides, resistive thermal sensors are positioned at the µLED pads, and the main thermal sensing circuits (e.g. OPA and buffer) are located at the frame head. A series of connecting pads are placed along the edge of the frame head, which are reserved for the connection with the second portion of this passive optrode. The second portion is the optrode patch (head-only). All operating circuits, including both local circuitries (µLED control, sensing, and recording) and global shared components, are compressed into the patch portion, and this optrode patch acts as a separate driving module for the passive T-shape frame. After fabrication, a post-bonding stage is needed to adhere these two portions together. Compared to the active configuration, this configuration costs more area, as no circuitry is slotted into the passive optrode shaft.

This subsection explores both active and passive configurations for optrode developments. The active design is an integral silicon-based optrode. It distributes all the local control & sensing blocks along the optrode shaft, whereas the passive version has a separate drive circuitry patch and passive bonding frame. A detailed comparison of these two versions is summarised in a radar chart in Figure 5.27.

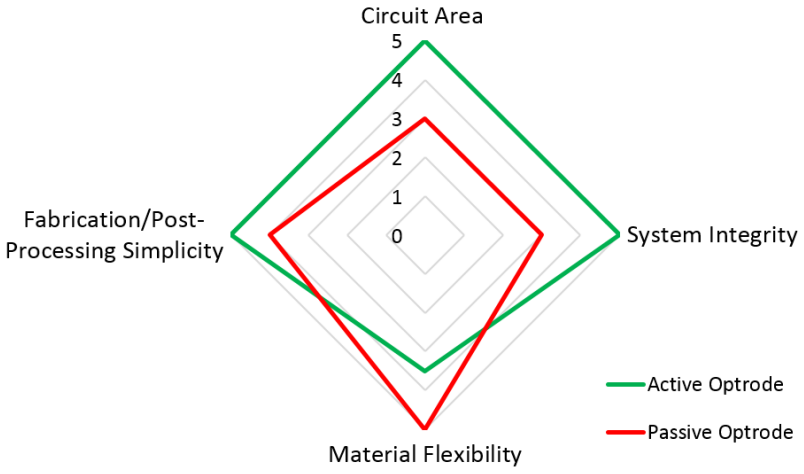


Figure 5.27 Radar chart comparing the major characteristics of these two different optrode configurations, in terms of circuit area, system integrity, material flexibility and fabrication/post-processing simplicity.

Regarding circuit area, the active optrode has better resource utilisation. This is because its local control & sensing circuits are placed next to each stimulation/recording site along the active optrode shaft, while the passive optrode requires a detached patch to include all the circuits without using the shaft area. Thus, the active configuration also leads to smaller dimensions and the lighter weight of the implant. Moreover, the active version represents better system integrity as it is constructed on a single piece of silicon rather than two separate portions. Then it can be directly cut as a whole T-shape. But the passive version needs additional chip-to-frame bonding processing. However, a limitation of the active optrode is its material flexibility. As the active optrode is an integral design, the substrate material can only be silicon; whereas the passive frame could be fabricated using other materials, and bonded to the CMOS patch afterwards.

In summary, both active and passive configurations have inherent strengths and weakness. Although the active optrode has limited material flexibility, it holds more advantages compared to the passive version, regarding circuit area, system integrity, device dimensions and post-processing techniques. These two optrodes have been both fabricated, and the overall performance will be further verified in future *in-vivo* tests.

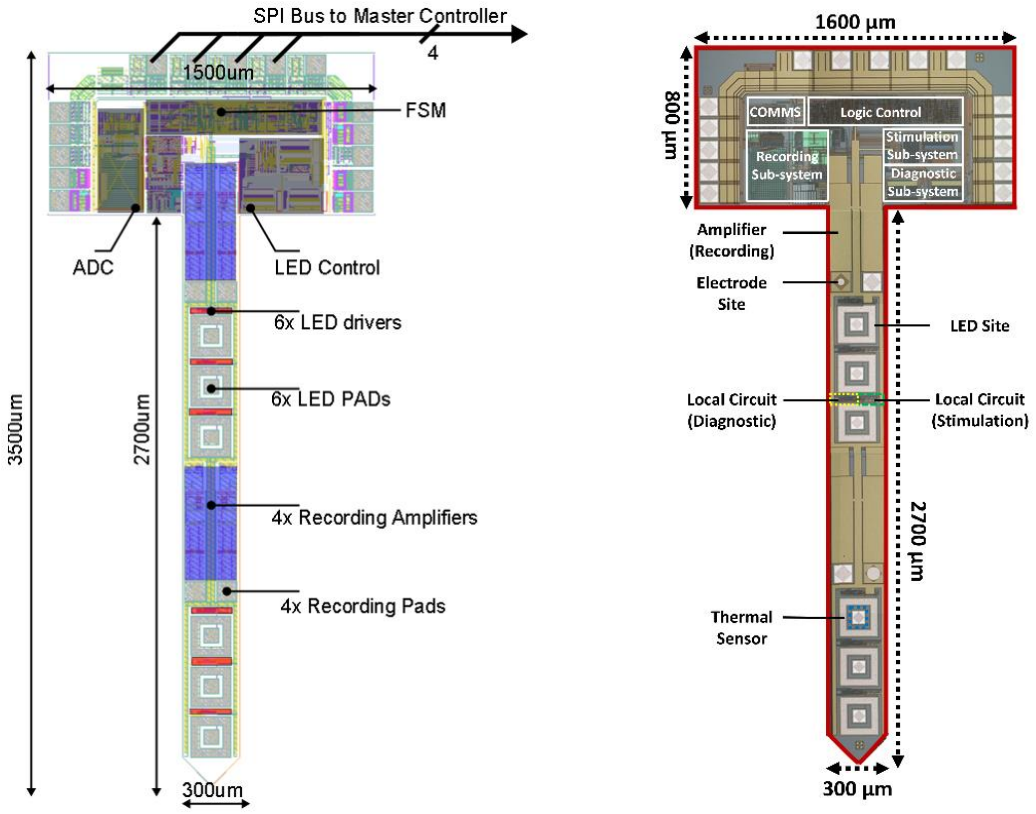
5.3.9 Chip Layout and Fabrication

The previous subsection detailed two different configurations of the closed-loop optrode. Both active and passive optrodes have been implemented and fabricated in an AMS 0.35-µm, 2-poly, 4-metal standard CMOS process.

Active Optrode

Figure 5.28 shows the layout of the active optrode. The total chip dimensions are 1600 µm × 3500 µm and the active die area is 1.96 mm^2. The size of the optrode head is 800 µm × 1600 µm, fitted with the floorplan proposed in Figure 5.19. The length of the optrode shaft is 2700 µm and its width is 300 µm. Similarly to the X-FAB optrode, the 300 µm shaft width contains three sections: the width of µLED bonding pad (190 µm), the width of metal wirings and spacing (35 µm on each side), and the perimeter margin (20 µm on each side). All local functioning circuits (optical stimulation, diagnostic sensing, and neural recording) are slotted into the shaft,

achieving direct local control and sensing. This also furthest minimises the total system dimensions.

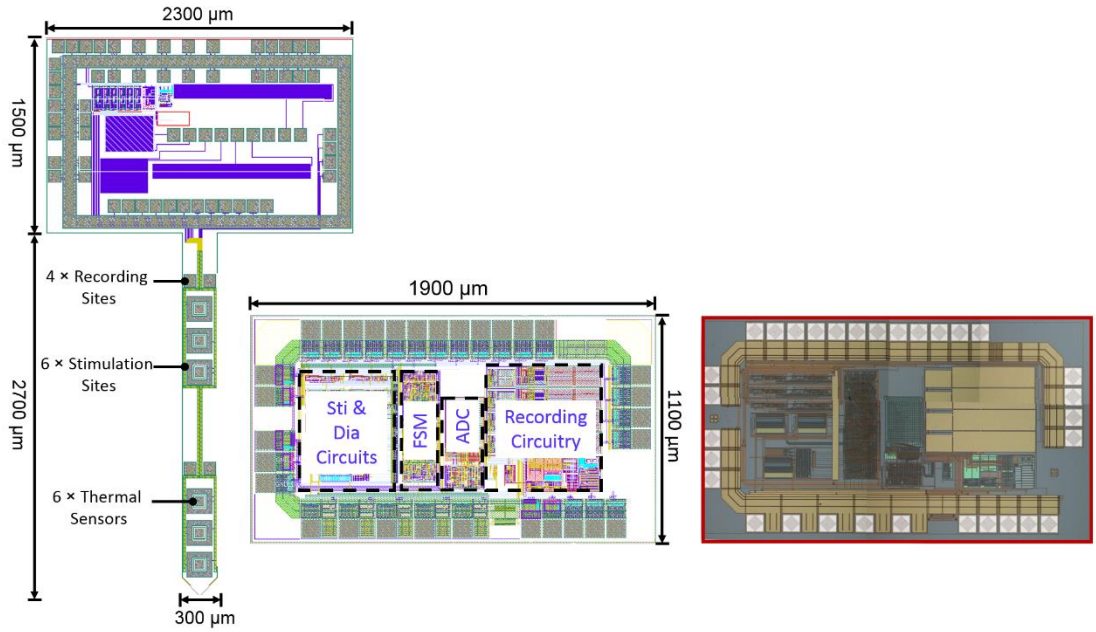


(a) (b)

Figure 5.28 (a) Layout diagram of the active optrode. All the local circuitries are placed in the optrode shaft. This fits with the system floorplan proposed in Figure 5.19. (b) Microphotograph of the active optrode.

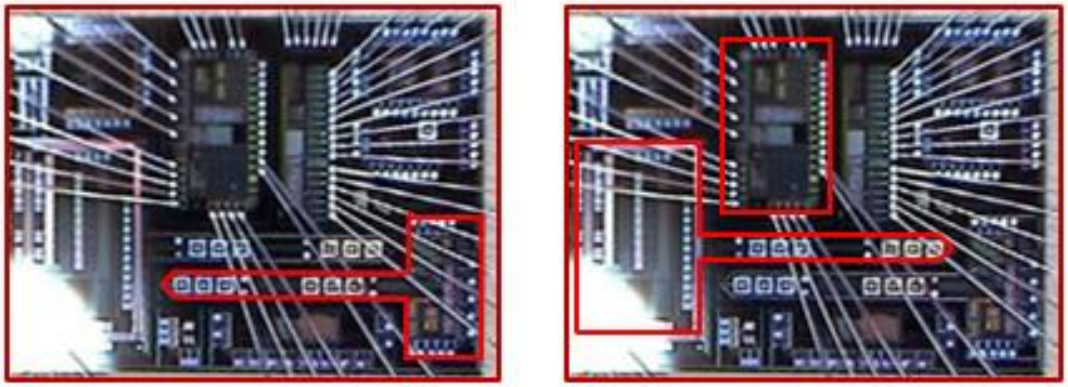
Passive Optrode

The layout diagram of the passive optrode is demonstrated in Figure 5.29. As mentioned above, it includes two main parts: the T-shape frame which includes all stimulation and recording bonding sites, and the optrode patch in which all the global and local circuitry is included. The total dimensions of the passive frame are 2300 µm × 4200 µm, with a 2300 µm × 1500 µm frame head. The optrode shaft is still 300 µm × 2700 µm, which is the same size as in the active optrode. The size of the passive optrode patch is 2300 µm × 1100 µm, and this could be directly fitted into the head of the passive frame. Compared to the active version, the passive optrode requires 60% additional area.



(a) (b)

Figure 5.29 (a) Layout diagram of the passive optrode. (Left) the passive frame of the optrode, including four recording sites, six stimulation sites and six thermal sensors. (Right) the patch part of the passive optrode, which contains all the global and local circuits of the optrode. (b) Microphotograph of the patch circuitry of the passive optrode.



(a) (b)

Figure 5.30 Microphotographs of a wire bonded chip die. (a) Active optrode. (b) Passive optrode.

The perimeters of both active probe and passive probe are sealed using scribe components to prevent leakage into the active devices and/or electrical connection, this also provides possible benefits for the fabrication process, such as deep reactive-ion etching (DRIE) and laser cutting. A schematic of this sealing ring is shown in Figure 5.31. Furthermore, the top metal layer (Metal 4) has been connected to the global ground as a cover to achieve further protection.

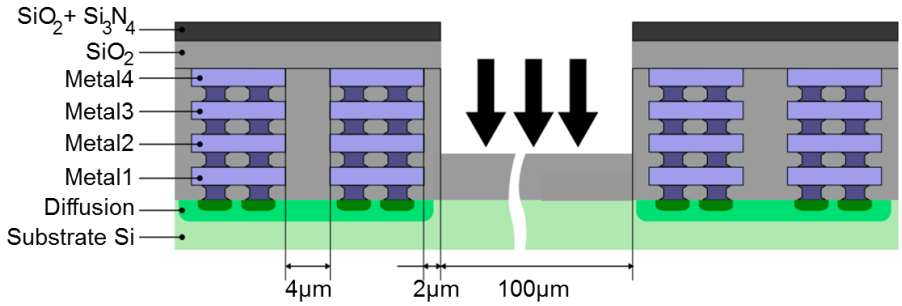
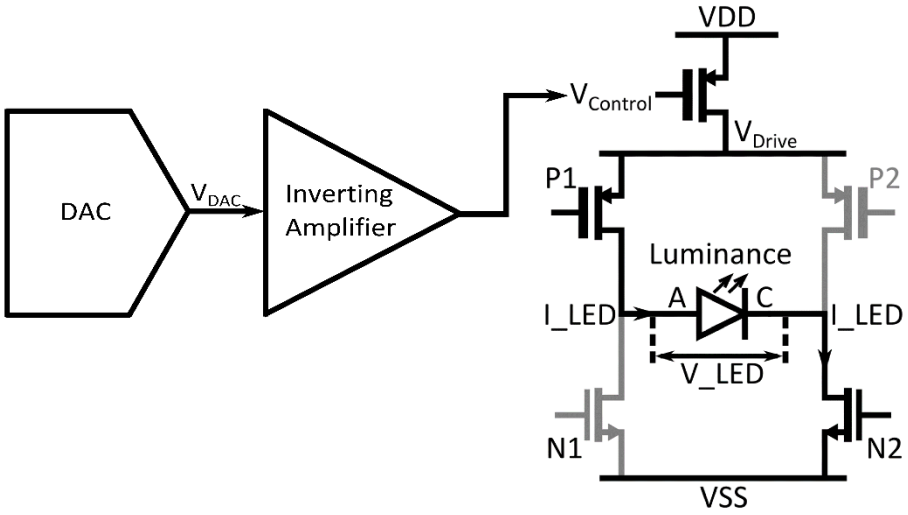


Figure 5.31 Scribe sealing for the optrode edge. The dimensions of each metal and insulator layer are referred the in process document [129].

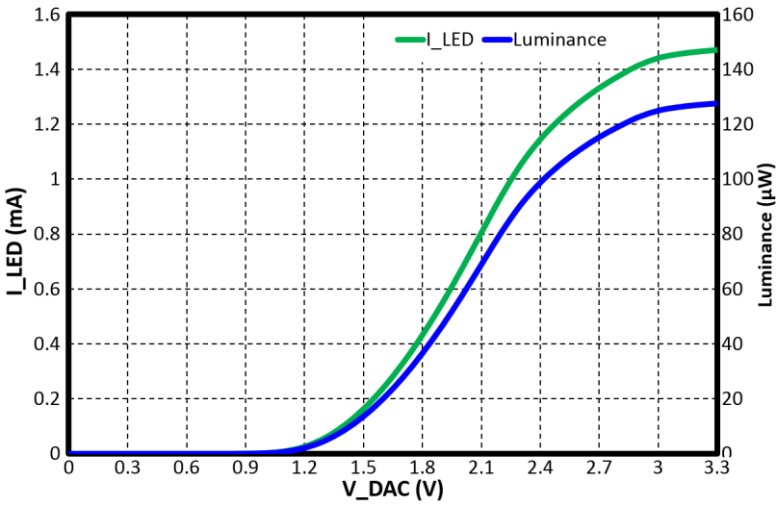
5.3.10 Top-level Simulation Results

Stimulation Control Function

Here, the functionality of the stimulation circuit is verified by top-level post-layout simulation. During optical stimulation operation, the μLED control voltage is generated by the 8-bit DAC and then converted into the corresponding drive current via the bi-phasic μLED driver. In this simulation, V_{DD_LED} is set as 5.0V, and the DAC input values is steadily adjusted from 0 V to 3.3 V to perform a scanning of the μLED current (I_{LED}) from 0 mA to 1.46 mA. The relationship between I_{LED} and V_{DAC} can be obtained correspondingly, as shown in Figure 5.32. Besides, the μLED luminance is deduced based on the μLED *I-V* curve and depicted below as well.



(a)

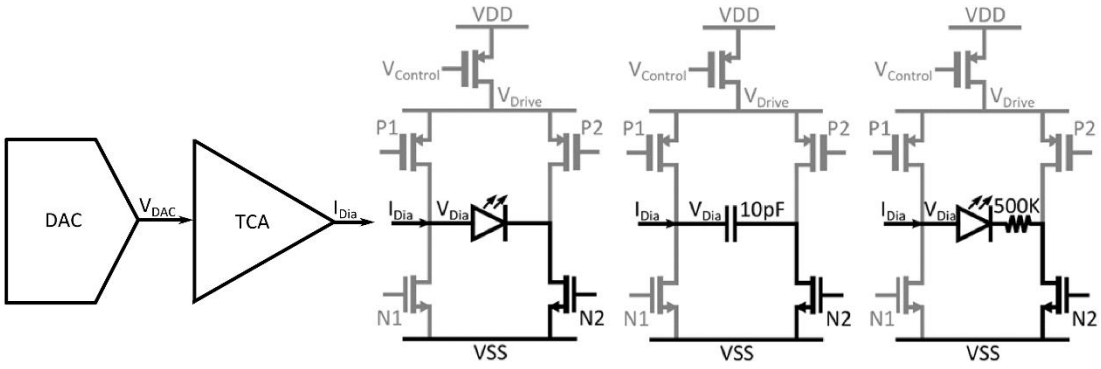


(b)

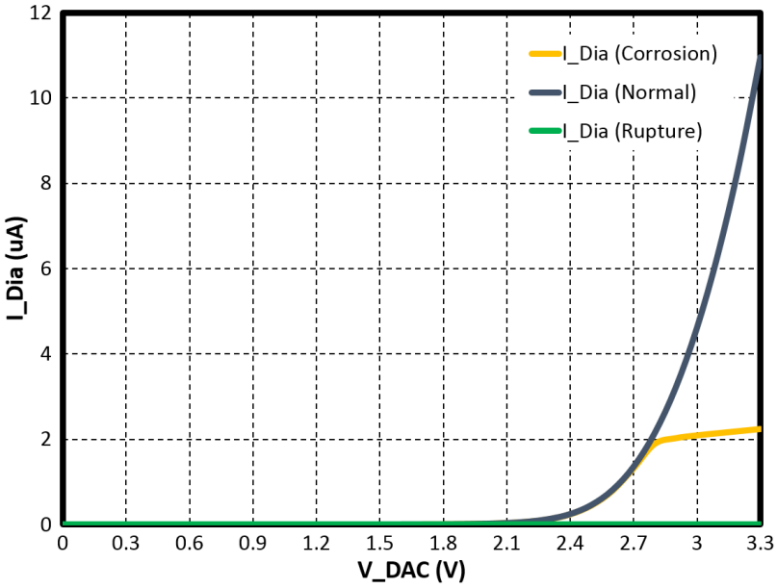
Figure 5.32 (a) Simplified equivalent circuit of the µLED stimulation circuit. (b) Correlations of I_{LED} versus V_{DAC} and luminance versus V_{DAC}. When V_{DAC} is 3.3 V, the maximum value of I_{LED} is 1.46 mA, and the corresponding maximum luminance is 128 µW. Global schematic is referred to Figure 5.21.

Diagnostic Sensing Function

Furthermore, a top-level post-layout simulation is also conducted to verify the performance of the diagnostic sensing circuit. As mentioned above, the voltage profile across the µLED would be different if the optrode is operating under different conditions, and this provides the feasibility of self-diagnosis analysis. In the diagnostic operation, the 8-bit DAC is used to define the input sensing voltage. This is then converted into a current expression via the TCA, to sense the targeted stimulation site. By tuning the input values of the DAC from 0 V to 3.3 V, a full-range self-diagnosis is achieved. As the diagnosis is performed at the dark region (where no light needs to be emitted), the diagnostic sensing circuitry could be powered by a 3.3 V power supply. In this simulation, three different optrode operation scenarios have been investigated: normal operation, shaft rupture, and contact erosion. Their current and voltage profiles are illustrated in Figure 5.33 and Figure 5.34, respectively.



(a) (b) (c)



(d)

Figure 5.33 (a) Simplified equivalent circuit of the normal operation state. (b) Simplified equivalent circuit of the optrode rupture state. A 10 pF capacitor is use to mimic the open circuit. (c) Simplified equivalent circuit of the contact corrosion state. A 500 KΩ resistor is serially connected to the LED to imitate the increased contact resistance. (d) Current profiles of the diagnostic sensing circuit with the optrode in different operation scenarios. When the optrode is operating normally, the diagnostic current I_{Dia} is increased from 0 µA to 11 µA, as expected. When bonding erosion occurs, due to the increased µLED serial resistance, the effective range of I_{Dia} is correspondingly shrunk to 0 - 2.2 µA. In the shaft rupture status, as an open circuit exists, I_{Dia} is approximately equal to zero. Global schematic is referred to Figure 5.22.

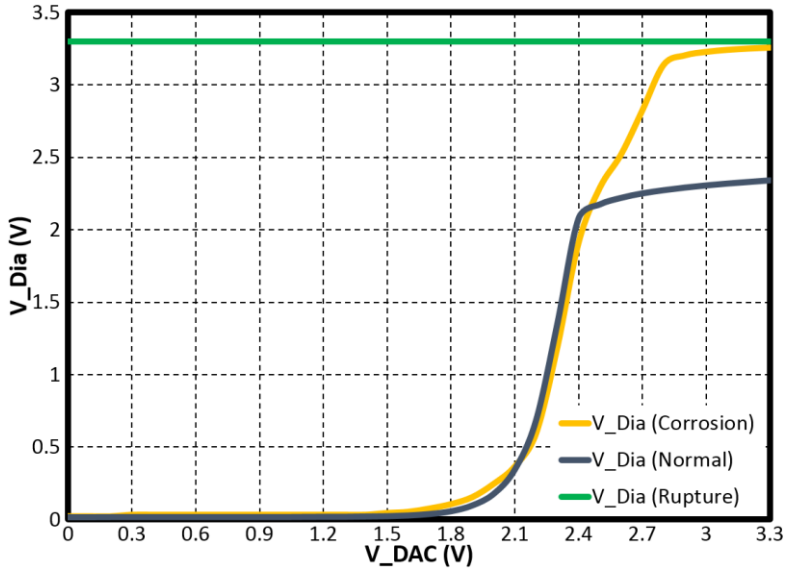


Figure 5.34 Voltage profiles of the diagnostic sensing circuit, with the optrode under different operation scenarios. When the optrode operates normally, the diagnostic voltage V_{Dia} is increased from 0 V to 2.33 V. When bonding erosion occurs, because of the increased µLED serial resistance, the active range of V_{Dia} is correspondingly increased from 0 to 3.26 V. In shaft rupture status, as an open circuit exists, the voltage is equal to the value of the power supply. Global schematic is referred to Figure 5.22, and equivalent circuit is referred to Figure 5.33.

It can be observed that, in various operation conditions, the characteristics of V_{Dia} are significantly distinct while sweeping the DAC input voltage (V_{DAC}). If the optrode is running in normal conditions, it performs a diode-like behaviour, and I_{Dia} is increased from 0 µA to 11 µA and V_{Dia} is changed from 0 V to 2.33 V. When an undesirable shaft rupture happens in the optrode, an open circuit is then created at the sensed stimulation site. Thus there is no effective current through the µLED, and the V_{Dia} is constantly equal to the power supply. In the contact corrosion situation, the serial resistance of the µLED is increased, which shrinks the I_{Dia} into the 0 - 2.2 µA range. The diagnostic voltage then rises from 0 V up to 3.26 V. In actual use, the targeted working range of V_{DAC} will be narrowed to 2.0-3.3 V, because the 3-state V_{DAC}-V_{Dia} profiles are profoundly different in that region, which makes the diagnosis operation more efficient.

Temperature Sensing Function

In this part, the performance of this resistive temperature sensor is proven by simulation. DC analysis is conducted to sweep the ambient temperature from 20 °C to 57.5 °C, and the result of the output voltage V_{Temp} is illustrated in Figure 5.35.

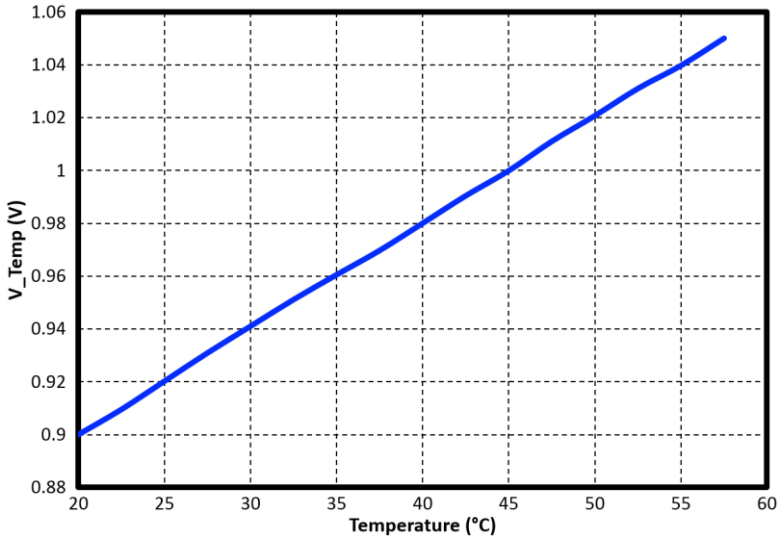
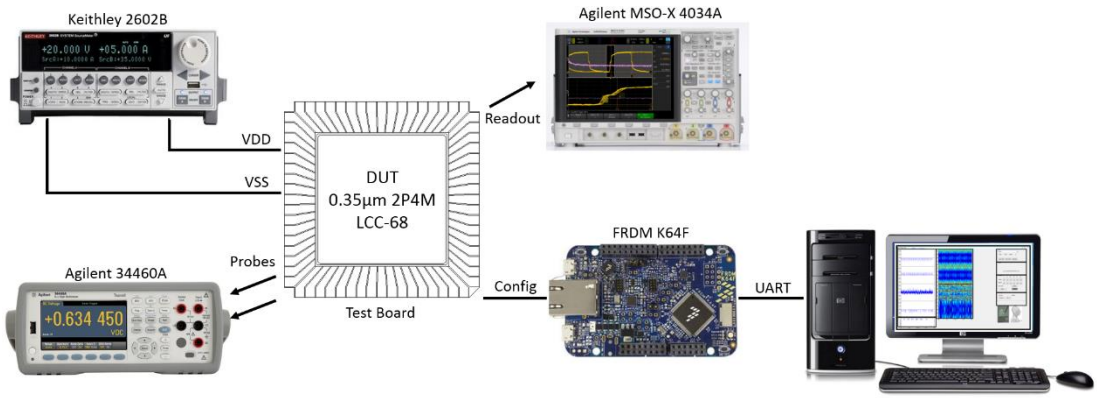


Figure 5.35 Relationship between the environmental temperature and output voltage change. V_{Temp} is gradually varied from 0.9 V to 1.05 V while the ambient temperature increases from 20 °C to 57.5 °C. The overall thermal sensitivity of this design is 4.0 mV/°C. Circuit schematic is referred to Figure 5.24.

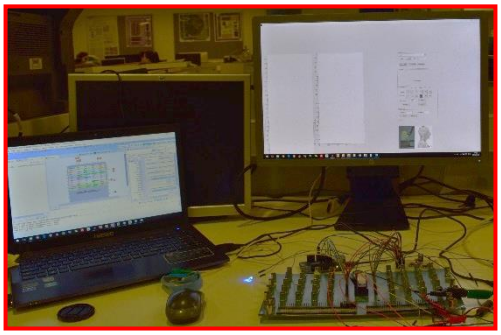
When the environmental temperature is risen from 20 °C to 57.5 °C, the output voltage V_{Temp} linearly increases from 0.9 V to 1.05 V. It can be observed that the temperature sensitivity of this sensor design is 4.0 mV/°C. Although this thermal sensor is relatively simple, it demonstrates a satisfactory linearity between the local temperature variation and the change of the output signal.

5.3.11 Experiment Set-up

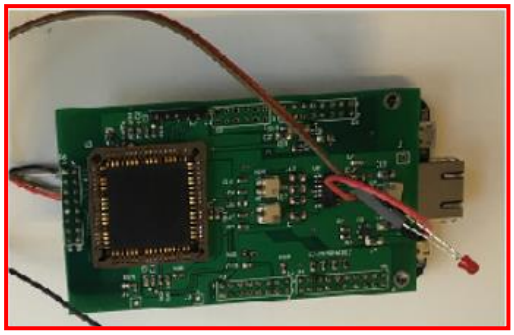
The general testing platform for this closed-loop optrode is shown in Figure 5.36. A Keithley 2602B source meter is utilised to provide both the 3.3 V and 5 V power signals and the global V_{SS}. A FRDM K64F microcontroller is utilised to configure and control the optrode chip package. An Agilent 34460A multimeter is applied to probe and record specific analogue signals (such as V_{LED}, and V_{Dia}), and an Agilent MSO-X 4034A oscilloscope is employed for time domain measurements. A MATLAB-based graphic user interface (GUI) is developed as a central user interface for commands initiations and data interpretations, and it communicates with the microcontroller unit via the UART (Universal Asynchronous Receiver/Transmitter) protocol.



(a)



(b)



(c)

Figure 5.36 Experiment set-up. (a) General testing platform for the closed-loop optrode design. (b) A FRDM K64 microcontroller-based testing platform, with measurement results captured by the MATLAB GUI. (c) Stack of the PCB and microcontroller platform, and the chip package is slotted into the dedicated PCB.

5.3.12 Measurement Results

Stimulation Control Function

This part focuses on the validation of the light driving ability. All measurements are conducted on the test bench displayed above. Input data are all generated by the FRDM-K64F board, and the global clock is set as 1 MHz, and the SPI clock MCLK is defined as 2 MHz. Power sources are provided by the Keithley 2602B for both analogue and digital domains. The input values of the DAC could be specified and updated via the MATLAB GUI.

A Panasonic µLED is selected for testing and then wire-connected to the µLED pads, and the current value I_{LED} through the µLED is captured by the sensing port of the Keithley 2602B. In the measurements, V_{DAC} and V_{DD_LED} are both adjusted in order to comprehensively investigate and verify the overall stimulation control function. In each measurement, V_{DAC} is tuned from 0.0 V to 3.3 V with 0.1 V steps,

and the V_{DD_LED} is set from 0.0 V to 5.0 V with 0.5 V steps for multi-round comparative measurements. Based on these settings, the measurement results of a single stimulation channel are illustrated in Figure 5.37.

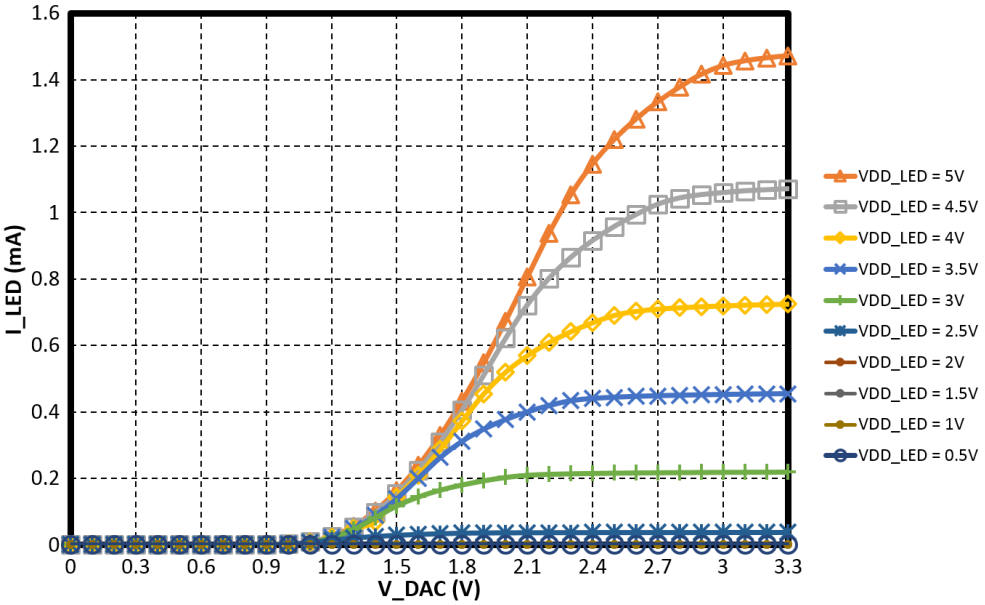


Figure 5.37 Correlations between I_{LED} and V_{DAC}. The V_{DAC} is set from 0.0 V to 3.3 V with a maximum of 256 steps. V_{DD_LED} is swept from 0.0 V to 5.0 V with 0.5 V steps, to investigate the light emission performance while applying variable power supplies. When V_{DD_LED} is restricted to 5.0 V, the maximum µLED driving current is 1.45 mA. Global schematic is referred to Figure 5.21, and equivalent circuit and top-level simulation results are referred to Figure 5.32.

It can be observed from Figure 5.37 that when the DAC is working in the 0-1.0 V range, there is no notable drive current. At this time, the µLED threshold is still not triggered. Once the input value of DAC rises beyond 1.0 V, the stimulation current then dramatically increases. Another observation is that when V_{DD_LED} is lower than 3.0 V, there is no significant drive current generated. This is because the voltage across the µLED is below its working threshold. When V_{DD_LED} becomes higher than 3.0 V, the µLED working threshold is reached, and a strong drive current is then created for light emissions. It could be noted that the current range is from 0.0 mA up to 1. 45 mA, which fulfils the design specification (0-1.35 mA for Panasonic µLEDs) proposed in Chapter 3. Besides, during the measurement, the voltage (V_{LED}) across the µLED terminals is also extracted, and the results are illustrated in Figure 5.38 below.

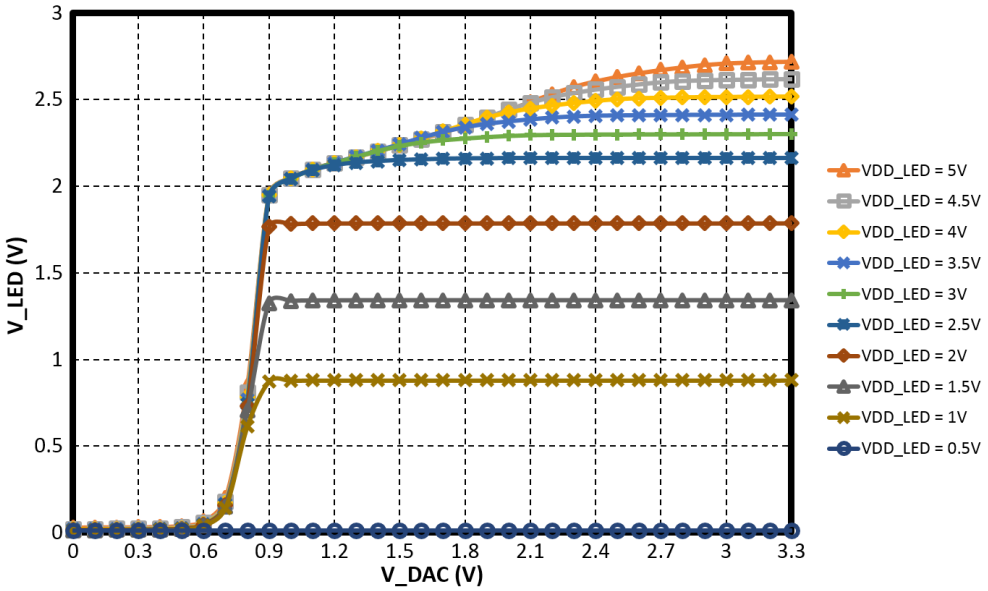


Figure 5.38 Relationship between V_{LED} and V_{DAC}. V_{DAC} and V_{DD_LED} keep the same settings. When V_{DD_LED} is equal to 5 V, the functioning range of V_{LED} is from 0.0 V up to 2.7 V as expected. Global schematic is referred to Figure 5.21, and equivalent circuit and top-level simulation results are referred to Figure 5.32.

It can be observed that, when V_{DD_LED} is lower than 3.0 V, with the increase of the V_{DAC} value, the V_{LED} correspondingly rises until saturating in the near region of $V_{DD\_LED.}$ This is because, when V_{LED} is below the µLED turn-on threshold, the light emitter is not active, and V_{LED} is mainly dominated by the parallel sheet resistance of the µLED. In this particular range, there is no significant current through the µLED. However, if V_{DD_LED} is equal to or greater than 3.0 V, then V_{LED} reaches the µLED working threshold, and drive current is subsequently produced. It can be seen that, when V_{DD_LED} is defined as 5 V, V_{LED} varies from 0 V to 2.7 V, and this range accords with the targeted drive voltage range specified in Chapter 3 (0 - 2.59 V for the Panasonic µLEDs).

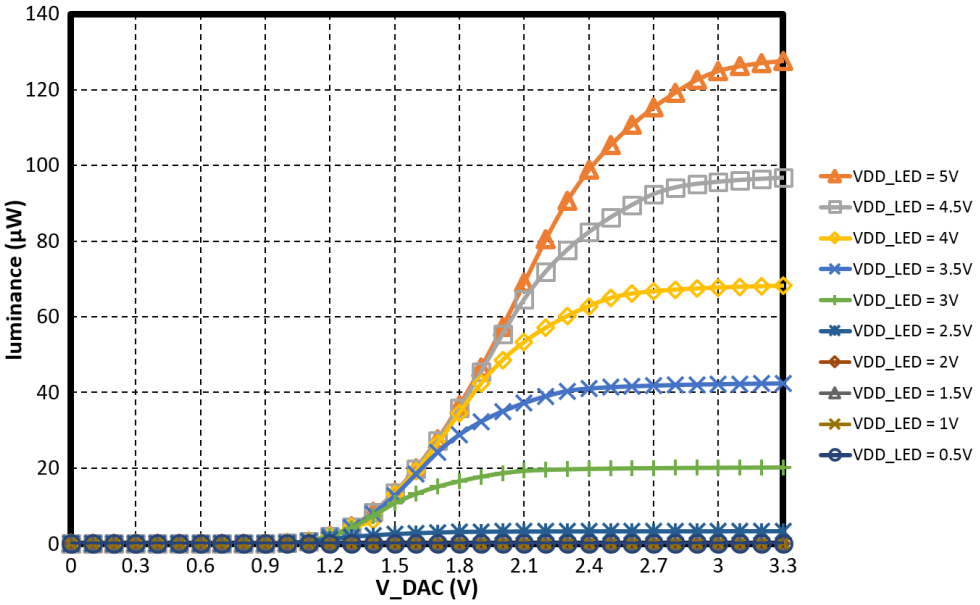


Figure 5.39 Correlation between luminance and V_{DAC}. V_{DAC} and V_{DD_LED} keep the same settings. When V_{DAC} is set to 3.3V and V_{DD_LED} is 5.0 V, the maximum luminance is 127.6 µw (deduced from Figure 3.8). Global schematic is referred to Figure 5.21, and equivalent circuit and top-level simulation results are referred to Figure 5.32.

Furthermore, based on the measurement results from Figure 5.37 and Figure 5.38, the luminance curve can be deducted, as shown in Figure 5.39. It can be seen that the luminance tracks the trend of I_{LED} while V_{LED} is controlled and constrained by the µLED drive circuitry. The maximum luminance is 127.6 µW when V_{DD_LED} is set to 5.0 V, and this result matches the previous global simulation result (128 µW) and fulfils the proposed design specification (≥ 105 µW).

In summary, this part has fully verified the stimulation control function by extracting the relationships among I_{LED}, V_{LED}, luminous intensity and V_{DAC}. The current and luminance driving ability of the stimulation circuitry are proven with satisfactory results. The experiments have also verified the light emission performance when the stimulation circuitry is given a variable power supply. More importantly, the light intensity could be regulated with 256 steps via the DAC, which ensures the resolution and accuracy of stimulation. This measurement proves that this stimulation control circuitry can produce targeted luminance with high modulation resolution, and thus achieves appropriate light driving ability and controllability. Therefore precise light emission and targeted penetration depth can be correspondingly accomplished.

Diagnostic Sensing Function

The optical stimulation function has been validated above with the expected results. In order to enhance system safety and robustness, the diagnostic sensing circuit has been incorporated within the optrode, and on-bench testing is performed to test its functionalities. As highlighted before, during the self-diagnosis procedure, the light emitter needs to be operated in 'dark' mode, and no light is allowed to be emitted. Therefore, a 3.3 V power supply is suitable for the diagnostic operation. Other aspects of the testing setups are the same as in the stimulation control tests.

Three different optrode operation scenarios, normal operation, shaft rupture and contact erosion, are investigated and compared. In the measurements, a regular Panasonic μLED is wire-connected to LED pads to construct the ideal operation condition. To imitate the shaft rupture situation, the regular μLED is replaced by a 10 pF capacitor, to mimic the open circuit of the optrode. And in the case of the contact erosion, the normal μLED is connected in serial with a 500 KΩ resistor to demonstrate a typical corrosion situation at the bonding site. By scanning the input value of the DAC from 0.0 V to 3.3 V, a corresponding sensing current I_{Dia} could then be generated under the different conditions. The comparative measurement results of I_{Dia} are shown in Figure 5.40, and the relationship between I_{Dia} and V_{DAC} is also illustrated.

It can be noted that, when the optrode is normally operating, the diagnostic sensing current is increased from 0.0 μA to 11.0 μA while V_{DAC} is swept from 0 V to 3.3 V. In contrast, for the contact corrosion status, because of the largely increased resistance between the light emitter and the CMOS circuitry, the sensing current is drastically decreased, and its active range is narrowed to 0.0 - 2.2 μA. For the shaft rupture state, because of the existence of the open circuit, the sensing current is at the fA level which is effectively negligible. These observations fit with the top-level simulation results shown in Figure 5.33.

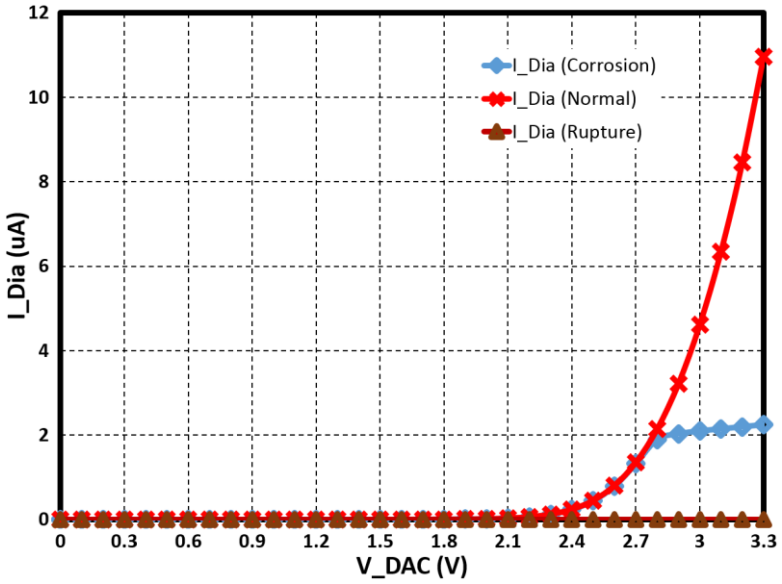


Figure 5.40 Correlations between V_{DAC} and I_{Dia} when the optrode is operated under three different situations. In the normal condition, the diagnostic current I_{Dia} is varied from in 0-11 µA range. When the optrode is working under the bonding erosion status, I_{Dia} is changed from 0 µA to 2.2 µA. When shaft rupture occurs, because of the existence of the open circuit, I_{Dia} is in the fA range. Global schematic is referred to Figure 5.22, and equivalent circuit and top-level simulation results are referred to Figure 5.33.

Once the diagnostic sensing current is generated, the diagnostic voltage V_{Dia} is subsequently created across the µLED anode. The measurement results of V_{Dia} from all three conditions are illustrated in Figure 5.41. It can be seen that, when the optrode is in the ideal state, the µLED performs a diode-like behaviour as expected. It finally reaches the transistor saturation region, and the maximum diagnostic voltage is saturated near to 2.36 V. For the bonding erosion situation, however, owing to the highly increased resistance, the original diode behaviour becomes more resistive. The output diagnostic voltage V_{Dia} dramatically increases to 3.28 V, and this corrosion abnormality could then be distinguished by recording the V_{Dia}. And in the final situation, as an open circuit is formed to the south of the sensing transistor, the diagnostic voltage is then constantly equivalent to the 3.3 V power supply. Thus, the V_{Dia} profiles are extracted and validated by on-bench measurements, and all these measurement outcomes precisely match with the previous top-level simulation results shown in Figure 5.34.

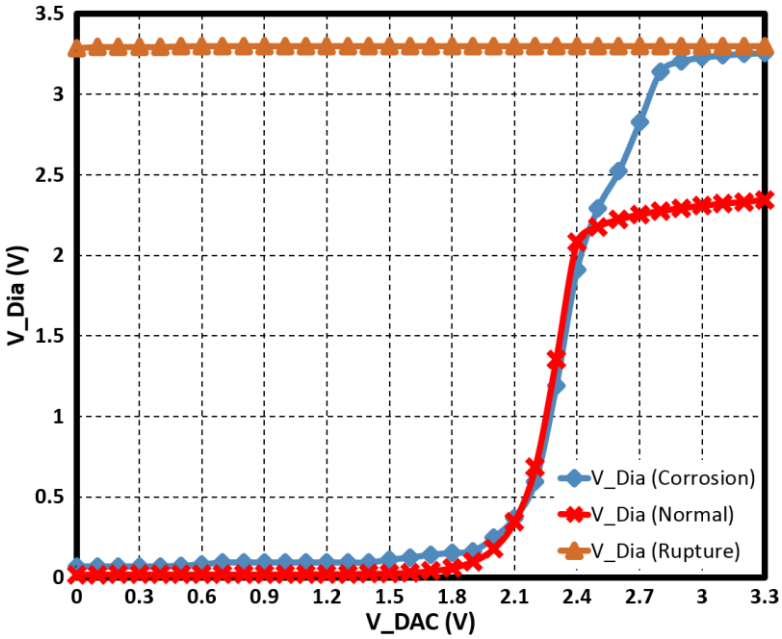


Figure 5.41 On-bench voltage profiles of the diagnostic sensing circuit, when the optrode is under different operation conditions. The V_{DAC} is adjusted from 0 V to 3.3 V. When the optrode is normally running, the V_{Dia} varies in the 0 - 2.36 V range. When bonding erosion occurs, the V_{Dia} is increased from 0 V up to 3.28 V. When the optrode is broken, V_{Dia} is equal to 3.3 V. Global schematic is referred to Figure 5.22, and equivalent circuit and top-level simulation results are referred to Figure 5.33 and Figure 5.34 respectively.

In particular, for the contact corrosion condition, the increased serial resistance would be variable depending on the level of degradation. In order to further analyse and verify the performance of the diagnostic sensing circuit, different values of resistors (from 100 Ω to 5.0 MΩ) are chosen to separately connect with the Panasonic µLED. This experiment demonstrates how the feature curves of I_{Dia}-V_{DAC} and V_{Dia}-V_{DAC} vary with different levels of contact corrosion, which provides more solid evidence for diagnosis analyses. The detailed experimental results are illustrated in Figure 5.42 and Figure 5.43. It can be noted that, when the bonding resistance is slightly increased (100 Ω), the performance of the µLED operation is basically not influenced, and this can be indicated by the profiles of I_{Dia} and V_{Dia}. If, however, there is a considerable rise of the resistance at the contact point, the expressions of I_{Dia} and V_{Dia} would then substantially differ from the initial feature curves. Thus, by observing the output value of V_{Dia}, the extent of contact corrosion could be deduced, and this will let the user or diagnostic technician determine whether to continue conducting the light emission or to switch to an alternate µLED or, in the worst case, to fully shut down the optrode.

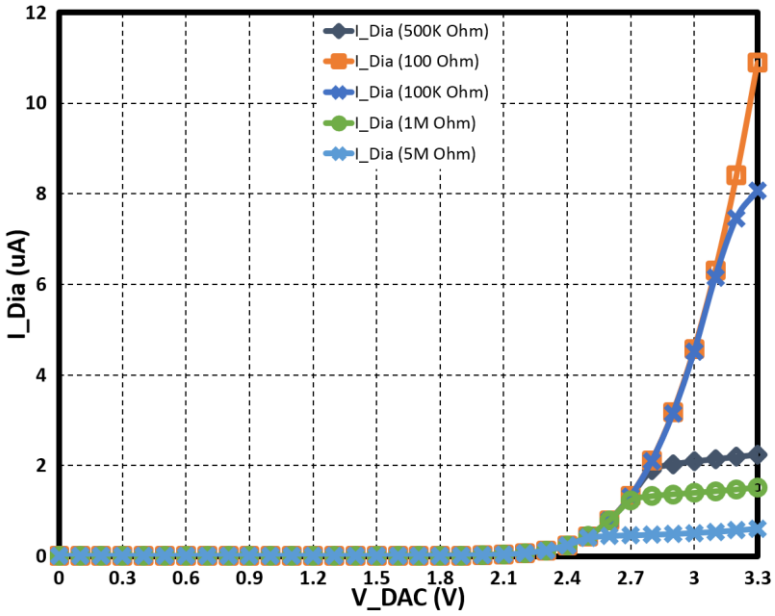


Figure 5.42 Correlations between V_{DAC} and I_{Dia}, and the bonding serial resistance is varied from 100 Ω to 5 MΩ. When the resistance is 100 Ω, there is a 0.1 µA reduction in the maximum I_{Dia}. With increases of the serial resistance, I_{Dia} is correspondingly decreases. When the resistance is set as 5 MΩ, the active range I_{Dia} is only 0-0.6 µA. Global schematic is referred to Figure 5.22, and equivalent circuit is referred to Figure 5.33.

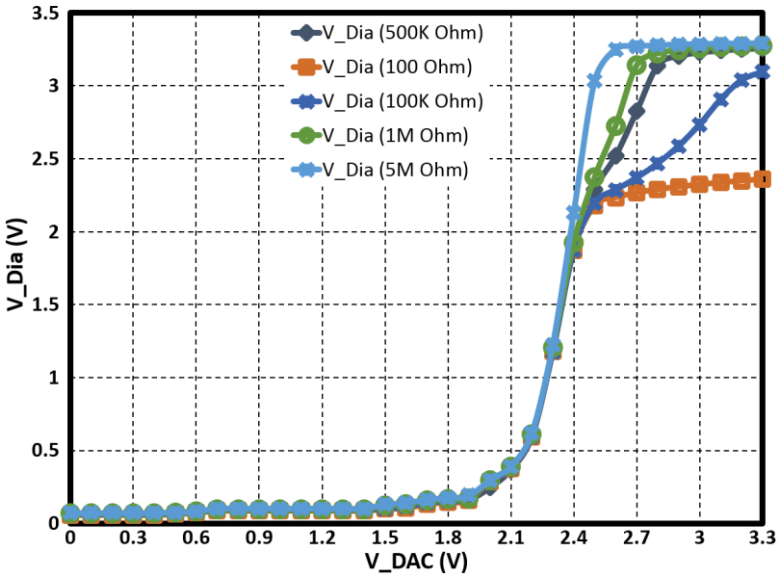


Figure 5.43 Correlations between V_{DAC} and V_{Dia} with variable serial resistance from 100 Ω to 5 MΩ. With 100 Ω serial resistance, there is a 0.15 V increase in the maximum V_{Dia}. The V_{Dia} is increased with the serial resistance. The V_{Dia} is saturated at 3.3 V when the resistance is set as 5 MΩ. Global schematic is referred to Figure 5.22, and equivalent circuit is referred to Figure 5.33.

In summary, the diagnostic sensing circuitry has been verified with the expected performance. Both the optrode breakage and bonding erosion situations are observed by the diagnostic sensing circuitry. In particular, the degradation level of the bonding sites is analysed in detail. This self-diagnosis function realises the real-time

abnormalities detection for optrode operations, which would significantly heighten the overall system safety and stability.

Temperature Sensing Function

After having fully validated both the stimulation and diagnostic functions, the functioning of the resistive temperature sensor is inspected on bench as well. A 3.3 V supply voltage is given for the LCC68 package by a linear power regulator, and the output of the sensing circuits is connected to the Agilent MSO-X 4034A. A sealed thermostat chamber is used to create a programmable temperature environment. The chip package and PCB are placed within the chamber. The temperature is increased firstly from 20 °C to 55 °C, with 5 °C linear steps, then decreased from 57.5 °C to 22.5 °C with the same steps. During each transition, the measurement was taken 20 minutes after the temperature reading of the chamber stabilised. The measured output voltage change for this temperature sensor is illustrated in Figure 5.44.

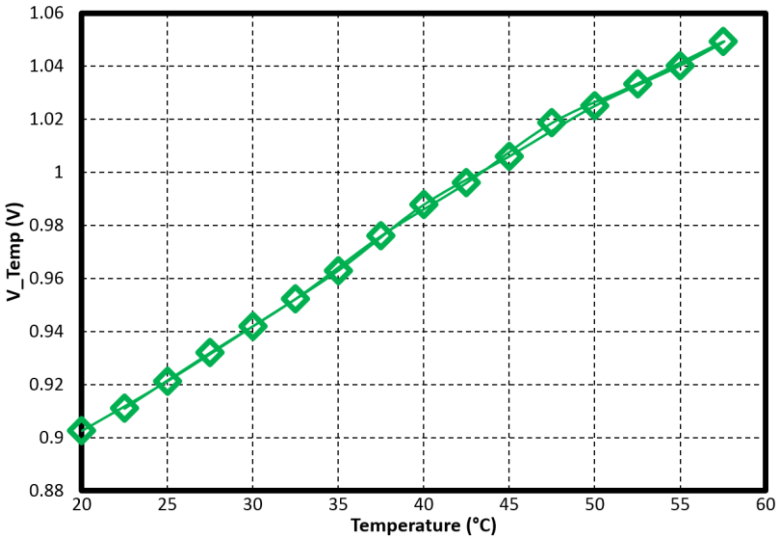


Figure 5.44 Measurement results of the resistive temperature sensor. The temperature is raised from 20 degrees to 55 degrees with 5 °C increment and then dropped from 57.5 degrees to 22.5 degrees with the same steps. The V_{Temp} is varied from 0.9026 V to 1.0492 V. The measured temperature sensitivity of this sensing circuitry is 3.91 mV/°C. These measurement results are provided by my colleague, Dr Yan Liu. Circuit schematic is referred to Figure 5.24. Simulation results are referred to Figure 5.35.

These measurement results illustrate a finer linearity of the *Temp-V* correlation. Based on the measurements, the overall temperature sensitivity is recorded as 3.91 mV/°C, fitting the simulation results in Figure 5.35, with only 2.25% difference. Besides, it can be observed that the hysteresis characterisation of this thermal sensor

is minimal. The overall performance of this resistive temperature sensor is summarised in Table 5.4. To conclude, this resistor-based temperature sensor is characterised with the anticipated results. It illustrates a well-behaved linearity and an acceptable overall sensitivity. These in-situ thermal sensing circuits could observe the thermal effects associated with the bonded light emitters after implantation and during normal operation, which further ensures both circuitry stability and tissue health.

Table 5.4 Performance summary the resistor-based temperature sensor.

Technology	AMS 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V
Active circuits area	600 µm × 200 µm
Sensing Core area	3100 µm × 0.6 µm
Total power	3.46 mW
Nonlinearity	0.27%
Sensitivity	3.91 mV/°C

Power Consumption

After all the verifications both in simulations and on-bench, the system power consumption of this closed-loop optrode is calculated and summarised in Table 5.5. It can be observed that when only one stimulation channel is active, the total system power consumption is 1.53 mW. Particularly, the light power is 362.5 µW. As previously mentioned (Chapter 3, Section 3.9), the defined system power budget is 14 mW and the continuous light power is 13 mW. Therefore, in practical application the optrode is capable to simultaneously switch on all six µLEDs, or (up to) eight optrodes can be concurrently operated with one active stimulation site.

Table 5.5 Total power consumption of the closed-loop optrode.

Subsystem	Major Circuits	Static power (μW)	Dynamic power (μW)	Utilised circuits duty cycle	Total Power (μW)
Logic control	FSM	0.00	10	100%	10
Optical stimulation	Pulse width modulator	0.00	$2.41\times10^{-3}\times2$	100%	4.82×10^{-3}
	Logic cells	0.00	2.5×10^{-3}	100%	2.5×10^{-3}
	DAC	260	260	5%	260
	Inverting amplifier	11.5		5%	0.575
	μLED	7.25×10^{3}		5%	362.5
	H-Bridge	0.1		5%	5×10^{-3}
Diagnostic sensing	Resistor string DAC	260	260	1%	260
	TCA	1.12		1%	0.0112
	Sensing transistor	12.7		1%	0.127
	SAR ADC	384	1.2×10^{3}	1%	392
Temperature sensor	Temperature sensor	3.46×10^{3}		1%	34.6
Recording circuitry	Recording circuitry	23×4	1.2×10^{3}	100% / 10%	212
Total Power (μW)		1532			

Although the total system power consumption is satisfactory, some limitations are still identified. In particular, the power consumptions of DACs and ADCs need to be largely improved in future.

5.3.13 Summary

In the previous subsections above, the implementation of all the subsystems of this optrode has been detailed, and all the optrode functions have been fully validated by both top-level simulations and on-bench experiments. The overall system performance is summarised in Table 5.6, and a comparative analysis between the current optrode and the previous optrode is conducted as well.

Table 5.6 Performance summary of this closed-loop optrode and comparison with the previous work.

System Overview		
	This work	The first version
Technology	AMS 0.35-µm, 2P4M CMOS	X-Fab 0.35-µm, 2P4M CMOS
Operation voltage	3.3 V, 5.0 V	3.5 (Min) - 5.0 V (Max)
Active circuits area	1.96 mm^2	0.13 mm^2
Total power	1.53 mW(1)/3.35 mW(6)	1.01 mW(1)/6.04 mW(6)
Optrode head dimensions	800 µm × 1600 µm	450 µm × 1000 µm
Optrode shaft dimensions	2700 µm × 300 µm	4400 µm × 200 µm
No. stimulation sites	6	6 (*3)
No. recording sites	4	N/A
Optical Stimulation		
µLED current range	0 - 1.45 mA	0 - 4.37 mA
Maximum luminance	127.6 µW	395 µW
Maximum light intensity	406.4 mW/mm^2	1256 mW/mm^2
Stimulation mode	Bi-direction	Mono-direction
Modulation methods	PWM, intensity control	PWM only
Diagnostic Sensing		
Input sensing current	0 - 11 µA	0 - 40 µA
Output diagnostic voltage	0 - 3.3 V	0 - 5.0 V
No. sampling points (Min)	14	4
Thermal Sensing		
Operational temperature range	20 °C to 57.5 °C	N/A
Output thermal sensing voltage	0.9 V to 1.05 V	N/A
Temperature sensitivity	3.91 mV/°C	N/A
LFP Recording		
Gain, PSRR	50 dB, 90 dB	N/A
ADC resolution, sampling rate	8-bit, 500 Hz	N/A

In this section, a closed-loop version of the proposed optrode is constructed and fabricated using an AMS 0.35-µm CMOS process. Six stimulation sites have been constructed and placed along the optrode shaft to realise multichannel neural stimulation. An intensity magnitude control scheme is created by employing an 8-bit DAC module. This provides an outstanding luminance controllability and ensures more accurate light delivery. This intensity magnitude control strategy could also minimise the over-heating hazard, confining the light power into a reasonable working range. Besides, the PWM mechanism is retained in this optrode design along with the intensity magnitude modulation, so as to attain satisfactory overall intensity modulations. Moreover, for the first time, a bi-directional µLED driver is formed to achieve biphasic light emission. This biphasic H-Bridge configuration can additionally be utilised to investigate the electrical characteristics of the reverse biased µLED in future explorations. Based on this structure, a µLED self-based temperature sensor is under development, and it could be applied in the future once the design is perfected. This H-Bridge is also configured for bidirectional diagnostic sensing. On the diagnostic side, higher-resolution data converters are incorporated to obtain more precise sensing results. In particular, the updated data converters require a much lower operational frequency, which is convenient for chip verification and practical use. This revised diagnostic sensing circuitry further guarantees operational safety and system durability. In addition, an in-situ resistor-based temperature sensor is developed to monitor the heating effect of the light emitters. These thermal sensors are placed within µLED pads, observing the real-time temperature on site. This thermal sensing design significantly heightens system robustness and, more importantly, makes sure of safe operation in brain tissue. Furthermore, external electrical neural recording circuitry is incorporated into this implant. This can observe concurrent local neural signals while the targeted neuron populations are photosensitized by the optical stimulator. By employing the recording subsystem, a closed-loop neural interface is completed. This neural processing platform could be widely utilised for diverse neurological disorders, such as Parkinson’s disease and epilepsy.

Compared to the first version of the optrode depicted in Section 5.2, this updated optrode design holds several advantages. This design can perform bidirectional stimulation whereas the previous version can only achieve mono-directional

operation. With the incorporation of the intensity magnitude control strategy, luminance controllability is considerably enhanced. By utilising higher-resolution low-frequency data converters, the precision of the self-diagnosis function is correspondingly heightened. Besides, in this new design, all individual control & sensing blocks are placed along the optrode shaft, and this configuration further minimises the area cost and assures the miniaturisation of the overall system.

However, although this new version demonstrates numerous merits, several flaws still exists. In contrast with the first version, the data converters used in the current design are relatively bulky. The actual area cost is 50 times that of the pulse-modulated DAC and ΣΔ ADC built into the first optrode. Thus, for this new optrode, to allocate data converters (both DAC and ADC) into each individual channel becomes impossible. These data converters are then placed in the optrode head as common components. The same arrangement applies for the Inverting Voltage Amplifier and TCA, which are also multiplexed by every channel. This setting might limit its future adoption in high-density μLED array development for visual prostheses. This also leads to a huge optrode head: 300% size of the previous one, which requires much more space for optrode placement and implantation. Additional weight is also added, and this may result in some discomfort and encumbrance for patients. Using a much larger die area (1500 % increment) also adds a considerable burden to the project costs. Moreover, due to utilising more complex circuits, only six μLEDs are positioned at this optrode shaft. Thus, the μLED clustering strategy cannot be adopted in this updated version, and backup μLEDs are not available. This might potentially decrease the durability of light emitters and weaken overall system robustness.

In this updated design, temperature sensors and neural recording circuitry are incorporated. Although these designs improve the system operational stability and add more new features for wider applications, there is still some room for improvements. Firstly, the resistive-based temperature sensor holds an overall sensitivity of 3.91 mV/°C. Although this is acceptable at this stage in exploring this multi-sensor CMOS optrode, its performance would need to be enhanced in the future. Circuit improvements can be made by placing localised sensing and amplification circuits, with advanced Proportional To Absolute Temperature (PTAT) circuits. Moreover, the area consumption of the neural recording circuits are

relatively massive. In particular, the FEA requires an area of 100 µm × 440 µm × 4 in the optrode shaft. Therefore, most of the components have to be positioned in the head part and shared by every channel. Additionally, in order to simplify the global control logic, each subsystem utilises separate data converters, and this increases the total area occupation in the optrode head. In future designs, these data converters need to be updated or replaced, and would be assigned for all subsystems.

5.4 Post-processing

The previous two sections have presented two versions of the optrodes, and three different configurations have been respectively implemented (including two active optrodes and one passive optrode). Post fabrication, to complete these neural implantable optrodes, relevant post-processing stages are required. A flowchart is displayed in Figure 5.45 to illustrate typical procedures in post-processing, and this work will be accomplished by the fabrication team of the CANDO project, at Newcastle University.

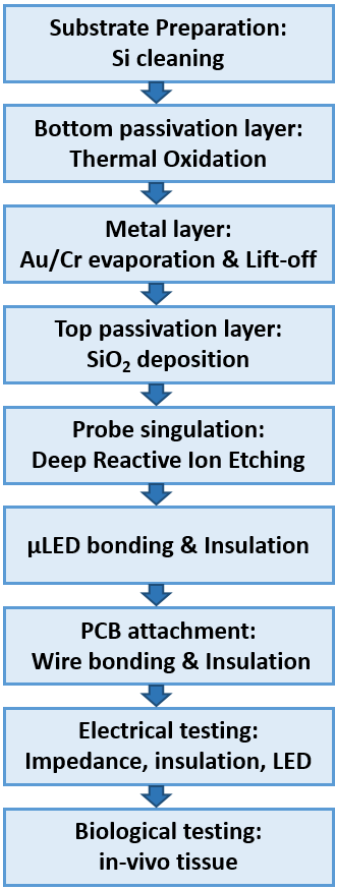


Figure 5.45 Required post-processing stages to complete optrode development. Once the targeted Tyndall µLED is in place, the optrode will then be verified experimentally, *in-vivo*.

5.5 Conclusion

This chapter has implemented two different versions of CMOS-based optogenetic implants. Diverse configurations have been explored and realised. Multi-site/multi-layer optical stimulation and precise local light delivery have been accomplished. Both monophasic and biphasic µLED drivers have been developed to generate the targeted strong current. PWM and intensity magnitude modulation have been created to obtain a satisfactory light intensity controllability. Besides, a self-diagnosis sensing scheme is created to assess optrode integrity and degradation in real-time. This approach has significantly heightened system reliability and operational safety. Moreover, in-situ resistive temperature sensors have been designed and placed within µLED pads to investigate the thermal effect of light emitters. This would be beneficial for both circuit operation and tissue health. Furthermore, electrical neural recording circuitry has been integrated into the optrode. Local neural signals could be simultaneously observed along with the optical stimulation actions. This could provide real-time feedback signals to the optical stimulation circuitry, so as to either trigger or inhibit the stimulation operation. It could also potentially improve the efficiency of optical emissions. The optrode has been fully verified on-bench and will be further validated experimentally, *in-vivo*. This integrated implantable optrode is expected to be a promising neural interface for wider neuroprosthesis applications.

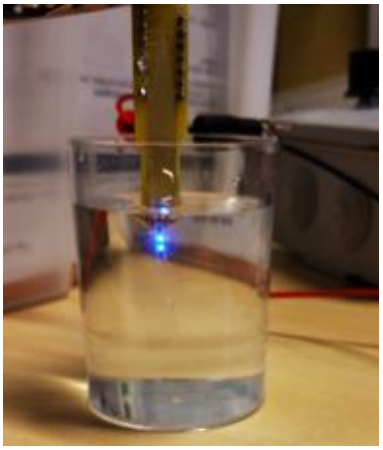


Figure 5.46 Fabricated optrode is operated under saline. Panasonic µLEDs are bonded on the optrode for initial testing. Further experiments will be conducted once the targeted Tyndall µLEDs are in place.

Chapter-5 Contributions

Contributor	Contributions
Mr Hubin Zhao	1) Defined the design floorplan of the optrodes 2) Developed and implemented the open-loop optrode 3) Verified and fully characterised the open-loop optrode 4) Developed and implemented the optical stimulation circuitry (independently), diagnostic sensing circuitry (independently), and the resistive temperature sensor (partially) of both active & passive of closed-loop optrode 5) Incorporated the external neural recording circuitry into the closed-loop optrode, and implemented the system integrations of both active & passive of closed-loop optrode 6) Verified and fully characterised the closed-loop optrode
Dr Yan Liu	1) Provided and trimmed the neural recording circuitry for the closed-loop optrode, in Figure 5.25 2) Provided the buffer and operational amplifier used in the resistive temperature sensor, and provided the measurement results of the resistive temperature sensor, in Figure 5.24 and Figure 5.44
CANDO Fabrication Team	Optrodes post-processing (in near future)

6 Conclusion

This thesis has presented a novel multifunctional optogenetic implant using a CMOS-driven GaN μLED approach. Different versions/configurations of optrodes have been implemented. Optical neural stimulation, electrical neural recording, self-diagnosis sensing, and local thermal monitoring have all been achieved within the fabricated optogenetic implants. This multi-sensor optical-electro neural interface aims to afford effective gene therapies for neurological disorders. It also provides a platform for neural engineers to explore broader applications in future.

This chapter firstly summarises the main original contributions of this work. Then potential future work is identified. The final part presents concluding remarks.

6.1 Original Contributions

Chapter 2 has introduced the basic knowledge and typical applications of neuroprosthetics and optogenetics. It has also explained why optogenetic stimulation is a novel tool for neuroprosthetics and how it can be utilised for neurological disorder therapies. Moreover, the state of the art of optogenetic implants has been reviewed. Wave-guiding structures and μLED-on-optrode approaches have both been introduced and compared, and their strengths and weaknesses have been respectively identified. Furthermore, based on the literature review of recently published work, the main development criteria for the proposed optrode have been deduced.

Chapter 3 has mainly depicted the design concept and major specifications of the proposed optogenetic implant. It has elaborated the relevant requirements from different points of view. From the perspective of biological application, the targeted penetration depth of light emission has been defined. The expected light driving ability has been subsequently identified. Moreover, the necessities for safety/durability evaluation and thermal management have also been pointed out. The fundamental principle of the self-diagnosis function has then been explained. In terms of device construction and manipulation, an intelligent active controlling method has been presented. A standard communication protocol (SPI) has been

supported for logic controlling and bi-directional data transmission. This controlling system is fully compatible with conventional biomedical μcontrollers, which can be utilised for wide-ranging applications. In addition, the commercially available 0.35 μm X-Fab/AMS CMOS processes have been chosen for optrode fabrications. This not only requires less cost and labour, but also provides a possibility for wider adoption and application. From the electronics design perspective, the requirement for finer luminance controllability has been highlighted, with benefits for both stimulation efficiency/accuracy and thermal management. In particular, a biphasic control pattern has been proposed for optical stimulation for the first time. This structure is configured for both optical stimulation and diagnostic sensing, and it will also be advantageous for future explorations. Besides, dedicated sensing circuitries have been demanded for real-time integrity/degradation assessment and thermal monitoring in the vicinity of each stimulation site. External electrical neural recording circuitry has also been required to be combined into the proposed implant.

Chapter 4 has detailed the electronic designs for both optical stimulation circuitry and diagnostic sensing circuitry. Diverse components have been designed, analysed and implemented. Some components have been commonly used for both the stimulation function and diagnostic operation, and the others have been dedicated to single operation. Monophasic and biphasic μLED drivers have both been implemented and compared. And the H-bridge structure has been created for optogenetic stimulation for the first time. This design has been helpful in the reduction of the degeneration by the electrical field during operations. It has also been beneficial for an on-going design of a μLED-based temperature sensor. A PWM method has been incorporated for light intensity modulation. Three types of pulse width modulators have been investigated and implemented. An intensity magnitude modulation scheme has also been created, and this has further enhanced the programmability of light emission. Diverse DAC designs have been proposed and achieved for μLED drive voltage/current adjustments. These structures have also been utilised to accomplish voltage/current scanning for diagnostic purposes. A 5-transistor step-up Inverting Voltage Amplifier has been developed to connect the standard 3.3 V circuitry with the 5 V μLED driver. Likewise, an 8-transistor step-up TCA has been formed in the diagnostic circuitry. It has transformed 0 - 3.3 V DAC input voltage into a 0 - 11 μA weak diagnostic sensing current, to perform the self-

diagnosis operation in ‘dark’ mode. This has saved energy and, more importantly, has effectively ensured patient safety. In the output part of the diagnostic sensing circuitry, an ADC module has been utilised to observe the diagnostic voltage behaviour. Two different ADC structures (SAR and ΣΔ) have both been explored and realised. In particular, the miniature ΣΔ ADC holds the potential to be applied into high-density μLED arrays for visual prostheses in the future. Additionally, supplementary elements, including S-to-P, P-to-S, level shifter, and accessory logic cells, have been incorporated to complete the system. These achievements provide a rich components library for optrode implementations.

Chapter 5 has demonstrated the implementation of two versions of the proposed optogenetic implant. Both open-loop and closed-loop optrodes have been realised. All versions of the optrodes have been configured with small dimensions and sharp tips, and this would be very helpful for minimising tissue damage caused by physical insertion. Six stimulation sites have been constructed and placed along the implant shaft. In particular, a μLED backup scheme has been created within the first optrode. Each three μLEDs have been configured as a μLED cluster at an appropriate cost of shaft area, and this clustering has considerably increased optrode robustness and long-term durability with adjustable stimulation area and light intensity. Optical stimulation circuitry has been achieved in both optrodes. Multi-site/multi-layer stimulation and targeted local light delivery have been attained. Both monophasic and biphasic μLED drivers have been explored and applied for μLED driving. PWM and intensity magnitude modulation methods have been utilised to render the luminance intensity highly programmable. This has not only improved stimulation operation accuracy/efficiency, but also helps in the thermal management of the optrode. Moreover, self-diagnosis function has been built into both implants. Three different operational scenarios (normal condition, optrode rupture, and contact corrosion) have been analysed, compared and validated. The integrity status and functional degradation of light emitters could then be observed in real-time. This diagnostic strategy has significantly enhanced system safety and long-term stability. Besides, local thermal sensors have been incorporated into the second optrode. These resistive temperature sensors have been positioned in the vicinity of each light emitter, monitoring local temperature rise. It has ensured both circuitry reliability and tissue safety. Furthermore, existing external electrical recording circuitry has been

imported into the second version design to construct a closed-loop neural implantable optrode. This can observe local neural activities and provide in-situ feedback signals for the optical stimulator. This has guaranteed the operation accuracy and efficiency of the stimulation function. In Particular, active and passive configurations have both been achieved for this closed-loop design. The active version has advantages in terms of circuit area, system integrity and post-processing. Meanwhile the passive version could be adaptable for other fabrication materials. Both active and passive optrodes will be further verified *in-vivo* tests in future.

6.2 Recommendations for Future Work

The suggested improvements for the technical contributions made in this thesis have been highlighted in each chapter, and so they are not repeated here. Thus, the focus of this section is to recognise potential directions and emerging technologies which would be meaningful for developments of the next-generation optogenetic implants.

Safety is always a key for implantable applications. As the optrode would be implanted into brain tissue, it is worthwhile to investigate the long-term moisture effects of the device. Humidity sensors could be explored and then integrated into future optrode designs. A possible way to do this is to measure the capacitance between the coating polymer layer and the CMOS top metal layer. Due to the influence of moisture effect, the relative permittivity of the optrode surface would be changed, which will induce variations in capacitance. By incorporating a capacitance to frequency converter, the humidity effect of the implant could then be observed. This humidity sensing strategy would further strengthen the system robustness. Another concern is about the material biocompatibility of the device. Although CMOS silicon is comparatively inert, it is sensible to cover the optrode with biocompatible coatings such as Parylene-C, to ensure that the implant has appropriate biocompatibility for the human body.

In terms of device miniaturisation, the circuit under pad (CUP) is a possible approach for chip area optimisation. Some local elements of both the stimulation circuitry and diagnostic circuitry could be placed underneath µLED pads. To achieve this, the stress effect for under-pad circuits should be investigated in the future.

The proposed optrode would be manipulated via a chest neuro-pacemaker, and this needs an appropriate link for power and data transmission. A four-wire system would be one option. In such four-wire transmission system, power/data transfer could be AC-coupled to avoid DC lead leakage in the case of lead breakage, and it can be fully-differential which cancel common mode noise and interferences. Two differential wires can be used for downlink data communication (commands from chest to optrode) and power transmission, and another two wires would provide uplink transmissions. In contrast, instead of using wire transmission, another choice is to utilise wireless communication technology. Wirelessly transmitting power/data could be more convenient for freely-moving animal experiments and clinical applications. Some initial work has been performed in our lab [116], and further researches are planned.

Regarding wider applications, the circuits developed in this thesis are not only suitable for optogenetic implants, but also adaptable for wearable high-density μLED arrays. The miniature pulse-modulated DAC and ΣΔ ADC in particular could be individually embedded into each array channel. SRAM cells could be utilised as pulse width modulators in matrix configurations. This high-density μLED array could be explored for future visual prosthesis applications.

Regarding the neural recording circuitry, apart from the electrical method adopted in this thesis, a new optical recording method could be explored in the future. Single-photon avalanche diode (SPAD) elements would be applied for optical neural recording, and could then be integrated with the reported optical stimulation circuitry to accomplish an optical stimulation-recording interface. The initial prototype has been fabricated, experiments and further improvements could be conducted in future projects.

6.3 Concluding Remarks

Optogenetics possesses great potential for treating neurological disorders. By photosensitising neurons via particular opsins, this method can be fully utilised for the investigation of complicated brain networks and neurological diseases. Potential applications are Parkinson's disease, epilepsy, blindness, and other conditions. One of the key challenges is to construct appropriate optogenetic implants to deliver local

light into the brain tissue of interest. This requires multidisciplinary effort from optical-electronics, biocompatible materials, precise fabrication, stable packaging, neuroscience and biology. Although different microfabrication techniques have been explored, no effective active electronics have yet been developed for optogenetic implants.

The work presented in this thesis has intended to investigate the interesting research question of how to develop a novel multi-functional optogenetic implant using a conventional commercially-available electronics design process. As the first prototype of the CMOS-based intelligent optogenetic implant, the proposed design will be a useful optical neuromodulation platform for the broad neuro-engineering community. The next five to ten years appears to be an exciting period for the development of new-generation optogenetic implants. I believe that this reported work will provide a solid base and effective contributions for future researches.

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Appendixes

A.1 Verilog-A Codes of LED Models

A.1.1 Verilog-A Code of Tyndall μLED

```
`include "discipline.h"
`include "constants.h"

//--------------------
// uLED model
//
// -  Based on Measurements
//
// vanode:        Anode voltage [V,A]
// vcathode:     Cathode voltage [V,A]
//
// INSTANCE parameters
//    {none}
//
// MODEL parameters
//    a, b

module LED(vp, vn);
inout vp, vn;
electrical vp, vn;
parameter real a = 0.297598017144345;
parameter real b = 5.159810114278211e-09;

  real vacross;

  analog begin
    vacross = V(vp, vn);
    I(vp,vn) <+ b*(limexp(vacross/a)-1);
  end
endmodule
```

A.1.2 Verilog-A Code of Panasonic µLED

```
`include "discipline.h"
`include "constants.h"

//--------------------
// uLED model
//
// -  Based on Measurements
//
// vanode:       Anode voltage [V,A]
// vcathode:     Cathode voltage [V,A]
//
// INSTANCE parameters
//    {none}
//
// MODEL parameters
//    a, b

module LED(vp, vn);
inout vp, vn;
electrical vp, vn;
parameter real a = 0.215177727563221;
parameter real b = 5.08425853519932e-09;

  real vacross;

  analog begin
    vacross = V(vp, vn);
    I(vp,vn) <+ b*(limexp(vacross/a)-1);
  end
endmodule
```

A.1.3 Verilog-A Code of Maplin LED

```
`include "discipline.h"
`include "constants.h"

//--------------------
// uLED model
//
// -  Based on Measurements
//
// vanode:       Anode voltage [V,A]
// vcathode:     Cathode voltage [V,A]
//
// INSTANCE parameters
//    {none}
//
// MODEL parameters
//    a, b

module LED(vp, vn);
inout vp, vn;
electrical vp, vn;
parameter real a = 0.218134256754369;
parameter real b = 3.47529005784878e-08;

  real vacross;

  analog begin
    vacross = V(vp, vn);
    I(vp,vn) <+ b*(limexp(vacross/a)-1);
  end
endmodule
```

A.2 SRAM-based Stimulation and Diagnostic Circuitry

Figure A shows a test circuit used to explore the SRAM-based stimulation and diagnostic circuitry. Biphasic µLED driver, amplification stages, and accessory logic cells are employed in this design. SRAM cells are functioning as pulse width modulators, along with dedicated SRAM drivers. These SRAM cells could be utilised in future high-density µLED arrays.

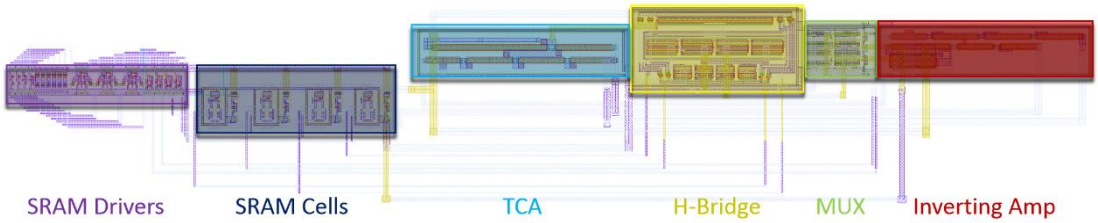


Figure A. Test circuits of SRAM-based stimulation and diagnostic circuitry. SRAM cells are used to act as pulse width modulators.

A.3 Single-Photon Avalanche Diode based Optrode

Figure B below demonstrates a SPAD based optrode (CANDO_v2) to explore an integrated optical stimulation-recording probe. Six stimulation sites are placed along the optrode shaft along with six SPAD cells. µLED control circuitry is constructed (by me) to perform optical stimulation while SPAD driving circuitry is developed (by my collaborator Mohammed Al-Rawhani at the University of Glasgow, UK) to conduct optical recording. This design provides the proof-of-concept of an optical stimulation-recording probe, experiments and future improvements could be conducted in the future.

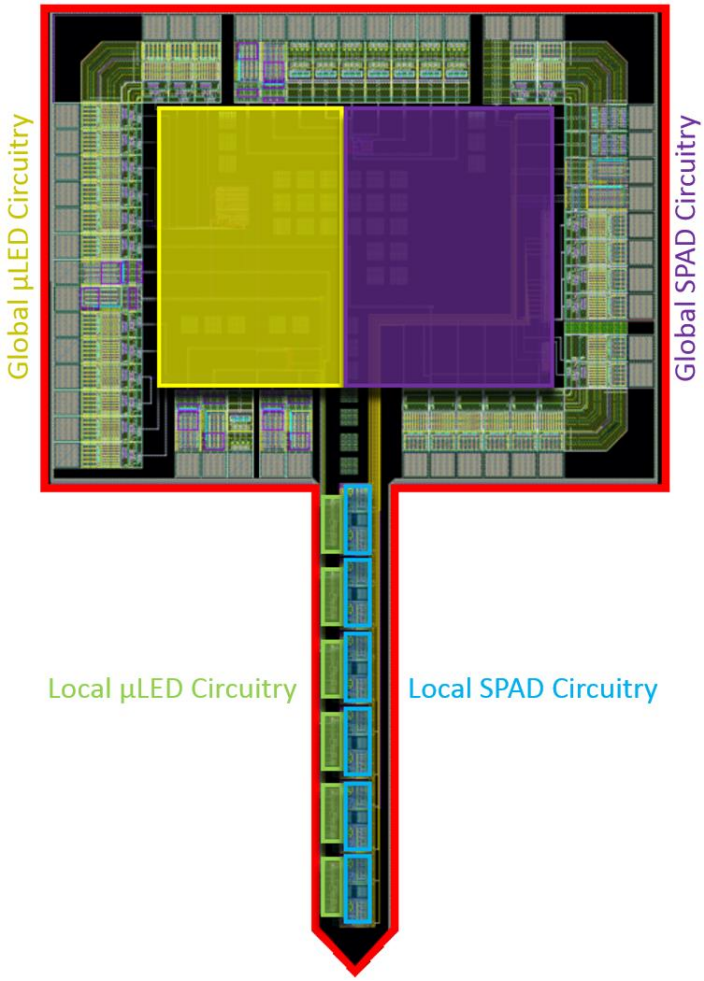
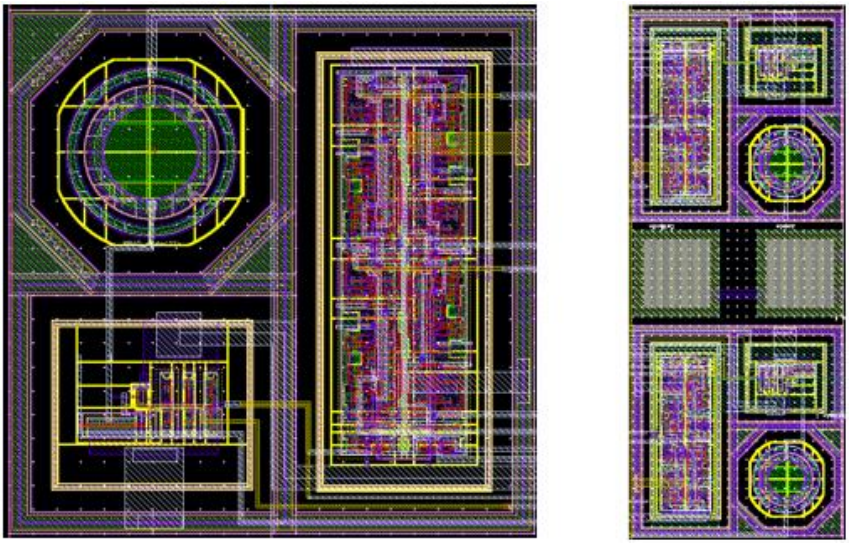


Figure B. SPAD-based optrode for optical stimulation and optical recording. Six SPAD cells are positioned in the vicinity of corresponding stimulation sites.



(a) (b)

Figure C. Layout of (a) one SPAD cell with an area of 110µm×100µm and (b) two SPAD cells placed in the vicinity of LED site. The SPAD cells are provided by collaborator Mohammed Al-Rawhani at the University of Glasgow.

A.4 µLED-based Temperature Sensor

Figure D shows a *Temperature-I* relationship of a reverse-biased µLED, and this result is based on the thermal measurement I conducted in 2014. It demonstrates a satisfactory linearity between the reverse current through the µLED and the environment temperature, when given a 2 V reverse voltage.

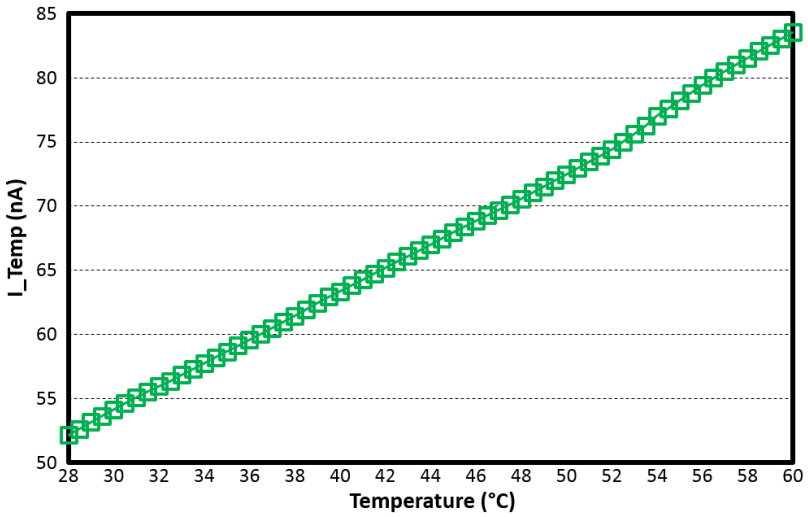


Figure D. Correlation between reverse current of the µLED and temperature when the applied reversed-biased voltage is (-) 2.0 V. The current I_{Temp} linearly varies from 52 nA to 84 nA when the temperature is changed from 28 ˚C to 60 ˚C, obtaining a sensitivity of 1 nA/˚C.

Based on this relationship, a µLED-based temperature sensor is proposed, as shown in Figure E below. Currently this sensor design is taken over by my colleague Dr Fahimeh Dehkhoda. Once the design is perfected, it can be integrated into future optrode designs.

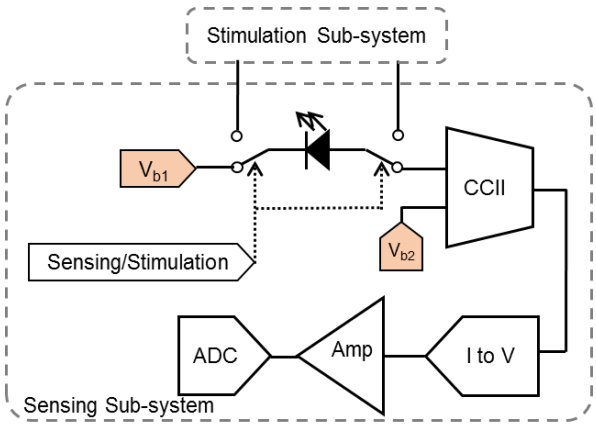


Figure E. µLED-based temperature sensor design. CCII circuit provides a fixed bias voltage (2 V) across the µLED and meanwhile transmit the reverse current to subsequent conversion and amplification stages for readout.

A.5 Micrograph of CANDO V1

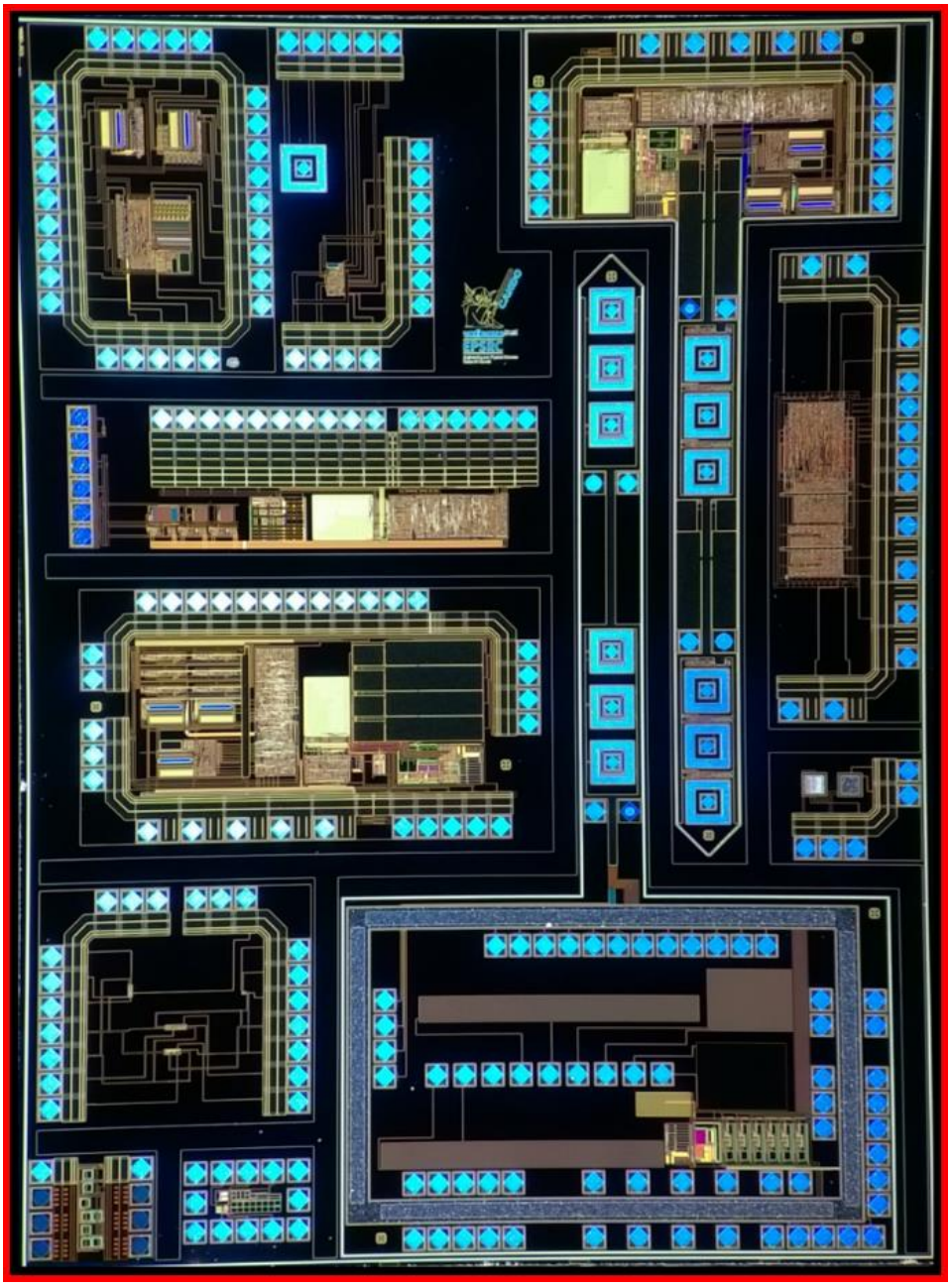


Figure F. Micrograph of CANDO V1. It includes both the active optrode and passive optrode (in Chapter 5, Section 5.3) along with relevant testing circuits.

A.6 Hubin's Face Reflected on X-FAB Wafer

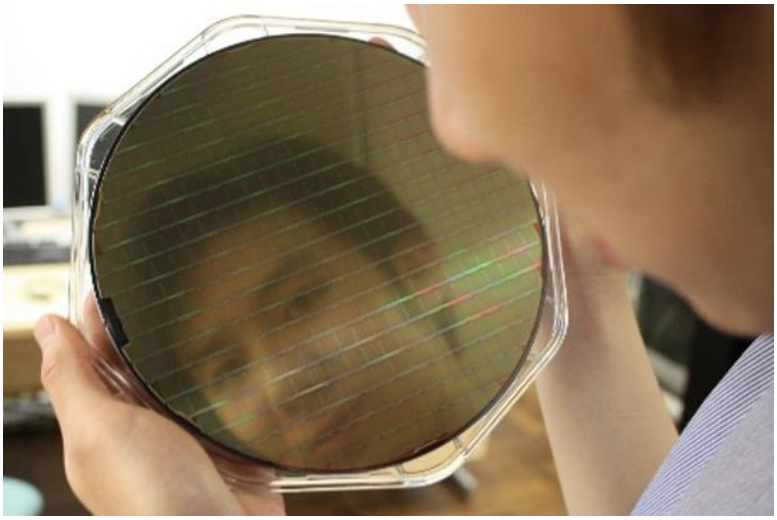


Figure G. My face is reflected on a 12" X-FAB wafer.

A.7 The Art of Metal and Poly

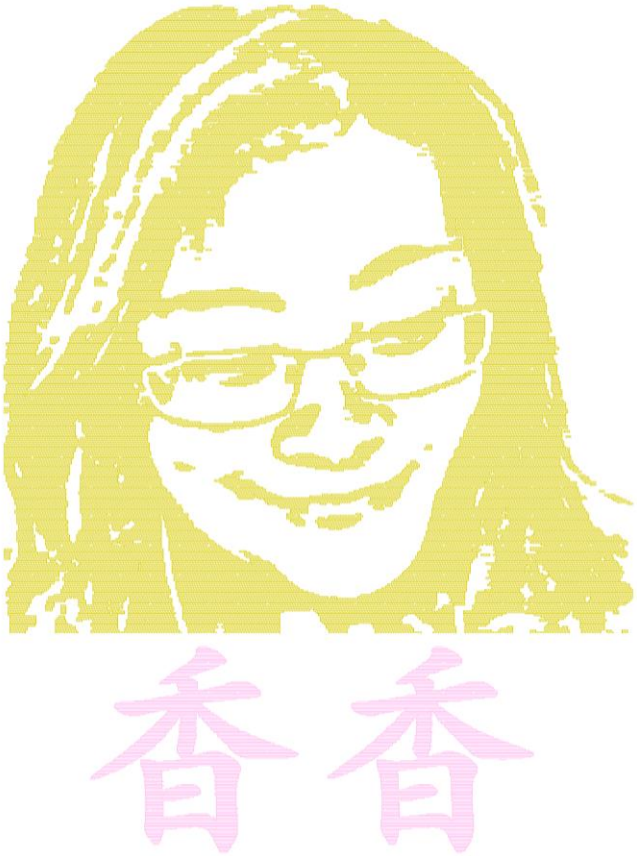


Figure H. The art of CMOS. My fiancée's face is designed using the Metal-3 layer of AMS C35B4 process. Her Chinese name is written using the Poly-2 layer.